MICROWAVE INTEGRATED CIRCUITS

Preparation of and measurement techniques for overlay capacitors

- by -

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March, 1974.

TEXT
CUT OFF IN THE
ORIGINAL

To
my parents.

ABSTRACT.

The work reported in this thesis is concerned with the fabrication and characterisation of microwave lumped element overlay capacitors for use at 10 GHz.

The research has included the investigation and selection of suitable materials for use in the component manufacture, and the development and optimisation of the necessary fabrication processes, which at the outset of the project, were not available to the author.

For this reason, and for the benefit of other research workers involved in the construction of microwave thin film components, the presentation of the processing data in this thesis is biased towards step-by-step accounts of each of the major processes. The processing data is then readily available in a practical, and useful, form.

Of particular interest in the processing field, is the novel technique developed for the deposition of the capacitor dielectric material without etching. This work was carried out in collaboration with a fellow research student, and is covered by a U.K. Patent.

The microwave measurement of the capacitor properties have been performed using microstrip resonators. To enable these measurements resonators to be accurately designed, measurements have been performed on, and results documented for, the transmission characteristics of microstrip lines on quartz substrates, and for the properties of microstrip gap discontinuities, and microstrip gap-and-step discontinuities, at X band.

The technique for the measurement of the overlay capacitor properties is novel in that the capacitor is measured "in situ", and bond wires, which are a characteristic of other measurement techniques, are not required. This permits a higher measurement accuracy, due to the reduction in connector parasitics.

In addition, the equivalent circuit approach to the calculation of the capacitor properties is used, and not the perturbation approach, which permits large changes in frequency and Q factor during the course of the measurements,

and this allows very accurate measurements to be obtained.

Results are presented for measurements performed on overlay capacitors, using silicon dioxide and alumina dielectric materials, and these indicate that capacitors with useful values of capacitance and Q factor can be produced at X band.

Theories are presented for the capacitor electrode inductance and resistance, and these enable the dielectric constant and Q factor of the capacitor dielectric materials, to be evaluated from the measured capacitor properties.

Values of the dielectric properties thus obtained are shown to be in good agreement with the characteristics of the dielectric materials in isolation, measured by a fellow research student, using cavity techniques.

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The work reported in this thesis is my own work unless credited, and it is not submitted at any other University. Some parts of the thesis have been, or will be, published in technical journals.

CONTENTS

1. INTRODUCTION

1.1 The development of Microwave Integrated Circuits.

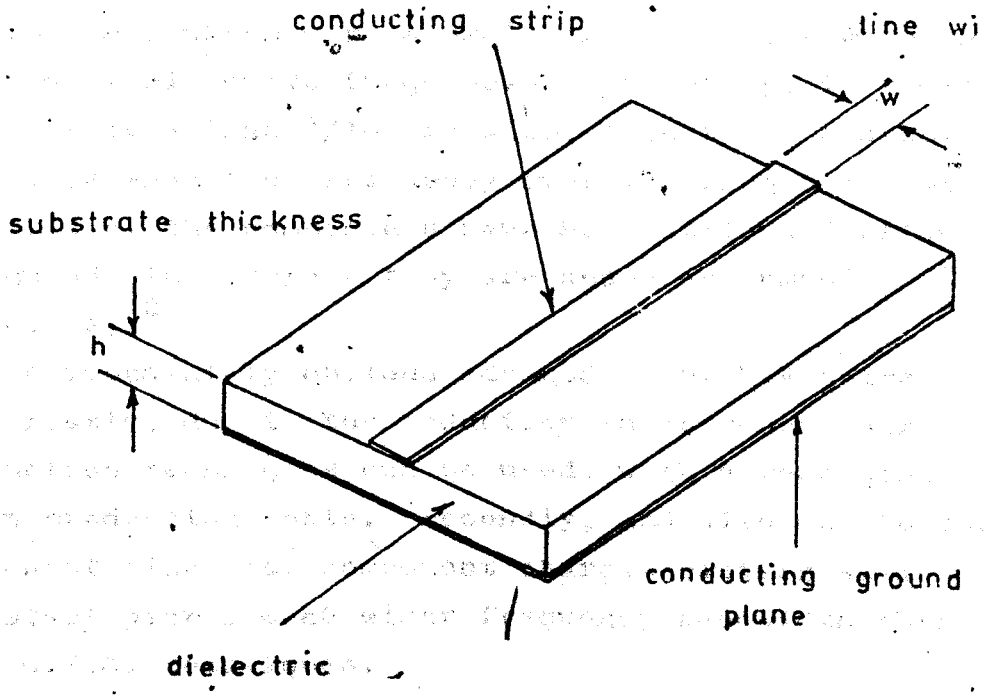
With the ever-increasing demands of the telecommunications and aerospace industries, there has been a continual requirement for electronic circuits to be made smaller, lighter and more reliable, and to operate at higher frequencies.

In recent years, one area which has received a great deal of attention is the microwave frequency range (1 - 20 GHz), which has traditionally been characterised by waveguide components, whose physical attributes of large size and weight are completely alien to the requirements of the aerospace industry.

At lower frequencies, these size and weight requirements have resulted in the development of the printed circuit board (p.c.b.), but at higher microwave frequencies, conventional p.c.b. components are comparable in size to a wavelength, and excessive losses and unwanted coupling prohibit their use. Manufacturing difficulties associated with the fabrication of very small components initially prevented the further miniaturisation of the p.c.b. devices to dimensions much less than a wavelength, which would have reduced these undesirable effects. Interest was therefore turned on an alternative approach, using "distributed circuits", in which transmission lines perform the functions of resistors, inductors and capacitors.

The most popular form of distributed circuit adopted for microwave integrated circuits (M.I.C's)[1] was microstrip line (figure 1.1), which consists of a conducting strip separated from a metallic ground plane by a dielectric sheet.

A factor which helped contribute to the widespread development of microstrip in M.I.C's was that all circuit definition is performed in the plane of the strip conductor, and, for a given substrate and frequency, the circuit parameters are determined simply by the width and length of the transmission lines.



Microstrip Line

Figure 1-1

However, the microstrip circuits exhibited low Q factors, and although they were considerably smaller than their waveguide or coaxial counterparts, they covered a comparatively large substrate area. For this reason, they could not be batch-produced using step-and-repeat techniques, and were therefore relatively expensive.

After thorough establishment of microstrip as a distributed circuit, developments in microcircuit processing technology in the semiconductor industry, made it possible to produce components which were a small fraction of a wavelength in size, even at microwave frequencies. Typically, if these components are less than $\lambda/100$ in size, then their characteristics are independent of frequency over the frequency range of interest. i.e. the components have no distributed effects and are "lumped" in nature - they are known as lumped elements (L.E's).[2]

The immediately obvious advantages of L.E's are twofold. Firstly, due to the reduction in component size, batch-production techniques can be used, with a resulting decrease in production costs. Secondly, and also due to the small component size, the component characteristics will remain constant over a much wider frequency bandwidth than with other M.I.C. techniques.

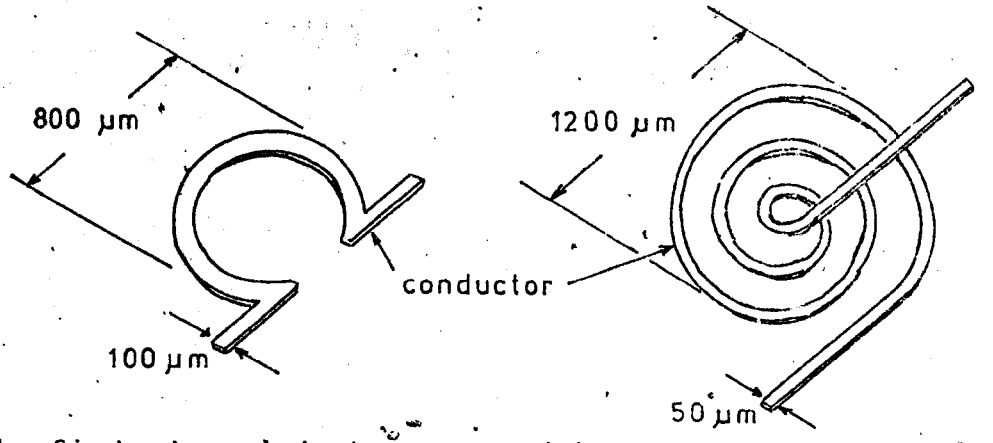
Some typical forms of practical L.E. inductors and capacitors and a resonant circuit are shown in figure 1.2, and an indication of the approximate sizes of the devices is also given.

The multiturn inductor is used for inductances above 1nH, which is the approximate practical upper limit for single turn inductors.

Although two forms of microwave capacitor are possible (i.e. interdigital and overlay), the applications to which they are suited are complementary.

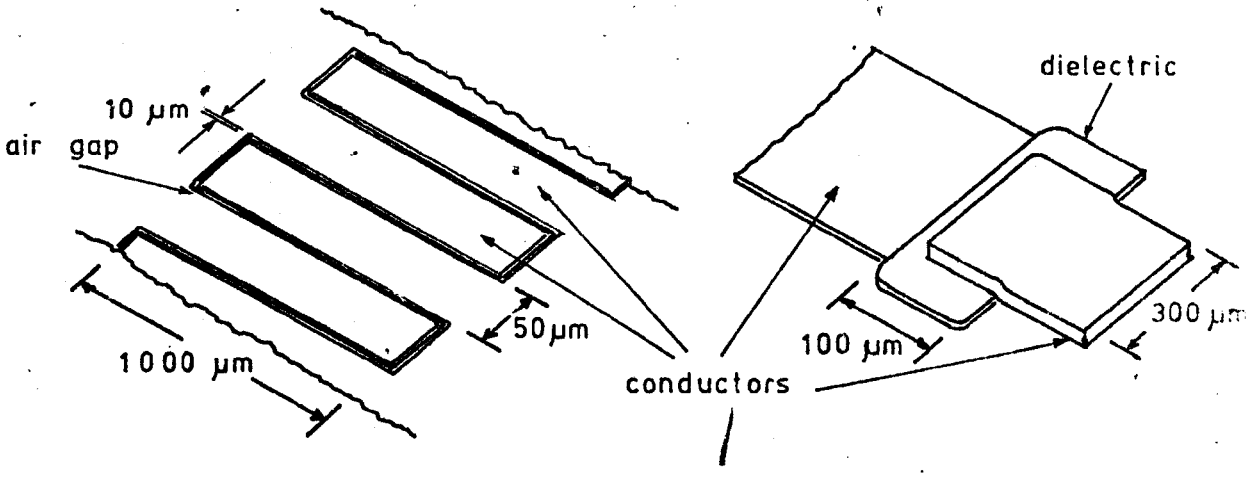
The interdigital capacitor[3-6] is a low capacity, high Q factor component, whose practical upper limit (which is limited by the component area and the introduction of distributed effects) is approximately 1pF.

The overlay capacitor is, on the other hand, a higher capacity, relatively low Q device, whose performance is limited



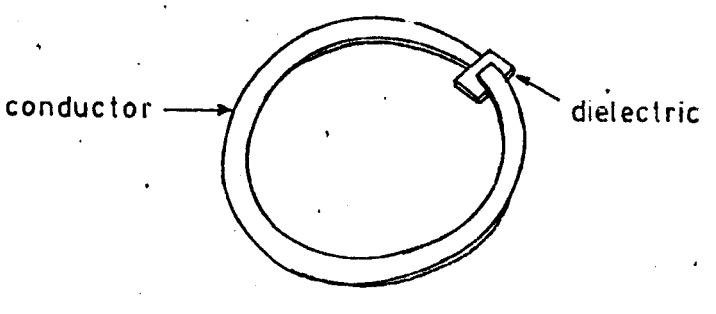
(a) Single turn inductor (b) Multiturn inductor

1. Lumped Inductors



(a) Interdigital capacitor (b) Overlay capacitor

2. Lumped Capacitors



3. Lumped Resonant Circuit

Figure 1.2 Lumped element components

at the practical lower limit of approximately 1pF, by the smallness in size and the resulting high resolution required from the processing technique. Another feature indicating the difference in the capacitor types is that the interdigital capacitor is a low cost device due to the simplicity of the structure, whereas the overlay capacitor, with its multilayer fabrication, is a high cost component, due to the increase in the number of processing stages.

Therefore, in practice, interdigital capacitors are used predominantly below 1pF at X band, and overlay capacitors used above this value.

1.2 Project objectives.

At Warwick University, a comprehensive research group has been established to investigate various aspects of M.I.C's, and the objectives of this particular project are closely related to, and complementary to, other topics being studied by the group.

The main group research topics are;

1. the investigation of the microwave properties of thin film conductor and dielectric materials.
2. the design and measurement of microwave capacitors.
3. the design and measurement of microwave inductors.
4. the computer correction of microwave measurements.
5. the computer-aided-design of M.I.C's.

The objectives of the project described in this thesis are;

1. the investigation and development of techniques for fabricating thin film overlay capacitors.
2. the development of a technique for the measurement of the characteristics of overlay capacitors at 10GHz, with particular attention being paid to the factors which contribute to the overall capacitor loss. (i.e. the dielectric and electrode losses).

In accordance with the above objectives, the ensuing discussion will be limited strictly to overlay capacitors operating at 10GHz, unless otherwise stated.

1.2.1 Detailed analysis of project objectives.

For the project to be of practical significance, the overlay capacitors investigated must be typical of those used in practical microwave circuit applications.

In chapter 1, therefore, a brief study of the various integration techniques of the L.E's with other M.I.C. components is given, as the adopted technique will determine the basic processing approaches permissible.

Then, having determined the integration technique to be used, the requirements of the materials to be used as substrates, conductors and dielectrics to optimise the component characteristics in this application are then investigated and the appropriate selections made.

An indication is also given in chapter 1 of the requirements of the manufacturing processes to produce the components, if the desired design requirements (e.g.tolerances) are to be achieved.

In chapter 2, the basic processing techniques adopted to attain these requirements are stated, and an indication of the extent to which the author was responsible in the construction of the equipment and the development of the techniques, is presented.

In chapter 7, the processing techniques adopted for the fabrication of thin film overlay capacitors are outlined, with particular emphasis being placed on the production of high Q elements, by techniques which allow a high processing yield with low capacitor tolerances. Of particular interest in this chapter is the novel technique devised for the deposition of the capacitor dielectric area.

As a result of the small dimensions of the overlay capacitors (typically 100 μm x 300 μm), and the large dimensions of the microwave test equipment used in the measurement of component properties, a suitable interconnecting feeder system is required to permit the physical and electrical compatibility

of the test gear and the components. Due to the basic form of the overlay capacitor, one type of feeder system which is particularly suitable, is microstrip line. To perform accurate measurements of the capacitor properties, the characteristics of the microstrip feeder system also require to be known to a very high degree of accuracy. Chapter 3, therefore, investigates the propagation characteristics of microstrip lines at X band, and Chapter 4 examines properties of various microstrip discontinuities, the characteristics of which were required to be known at a later stage in the project.

The theory of the measurement technique developed by the author for the measurement of the characteristics of microwave overlay capacitors, is then described in considerable detail in Chapter 5, and the complete measurement procedure is given in Chapter 8. Extensive design data for the technique is quoted, and results of investigations to verify the accuracy of the technique, by computer simulation, are also given in Chapter 8.

In Chapter 6, the relationship between the dielectric loss, the electrode loss, and the capacitor Q factor is investigated, and the influence of the electrode configuration on the Q factor is also considered. Results of scaled model experiments indicate, in particular, the effects of the electrode configuration and loss on the capacitor Q factor, and suggest possible electrode configurations to minimise component losses.

Chapter 9 then presents the results of measurements on a number of microwave overlay capacitors using the technique described in Chapter 5. The capacitor dielectric materials investigated are silicon dioxide (SiO_2) and alumina (Al_2O_3), and in the former case, the effect of varying electrode configurations and thicknesses on the final capacitor properties are investigated. The results are also compared with data obtained independently by Butlin[7] on measurements of the dielectric loss and conductor loss of the capacitor materials in isolation.

Chapter 10 then summarises the main conclusions of the project and briefly indicates possible future research projects which, in the light of the conclusions drawn from work in

this thesis, may prove to be of significance.

1.3 Lumped Elements - their advantages and disadvantages.

A comparison of the main characteristics of L.E's with other forms of conventional M.I.C's is given in figure 1.3, which lists the techniques, and their qualities, in order of preference (1 = optimum technique).

The major advantages of L.E's are;

1. the physical size of L.E. components is considerably smaller than other forms of M.I.C. devices. It can be seen from figure 1.4, which shows the relative areas required for both distributed and L.E. overlay capacitors using common M.I.C. substrates and capacitor dielectric materials, that for typical values of capacitance required at X band, a L.E. overlay capacitor is approximately 100 times smaller than the corresponding distributed element. The space-saving of L.E's compared with coaxial and waveguide components is, of course, considerably greater. Consequently, a large number of devices can be fabricated simultaneously on one substrate, and therefore the cost of L.E. circuits tends to be lower that that of distributed circuits.
2. the component characteristics are constant with frequency over a relatively large bandwidth, whereas distributed circuits have multiple resonances which limit their operating range.

It has been shown (Appendix 1.1)[3] that the bandwidth of L.E. circuits is always equal to, or greater than, the bandwidth of the corresponding distributed circuit, and the ratio of distributed circuit bandwidth to L.E. circuit bandwidth for a capacitor in a resonant circuit, is given by

$$\frac{\Delta f_{DE}}{\Delta f_{LE}} = \frac{2}{1 + \dfrac{2 \arctan \omega C Z_o}{\sin 2(\arctan \omega C Z_o)}} \qquad 1.1$$

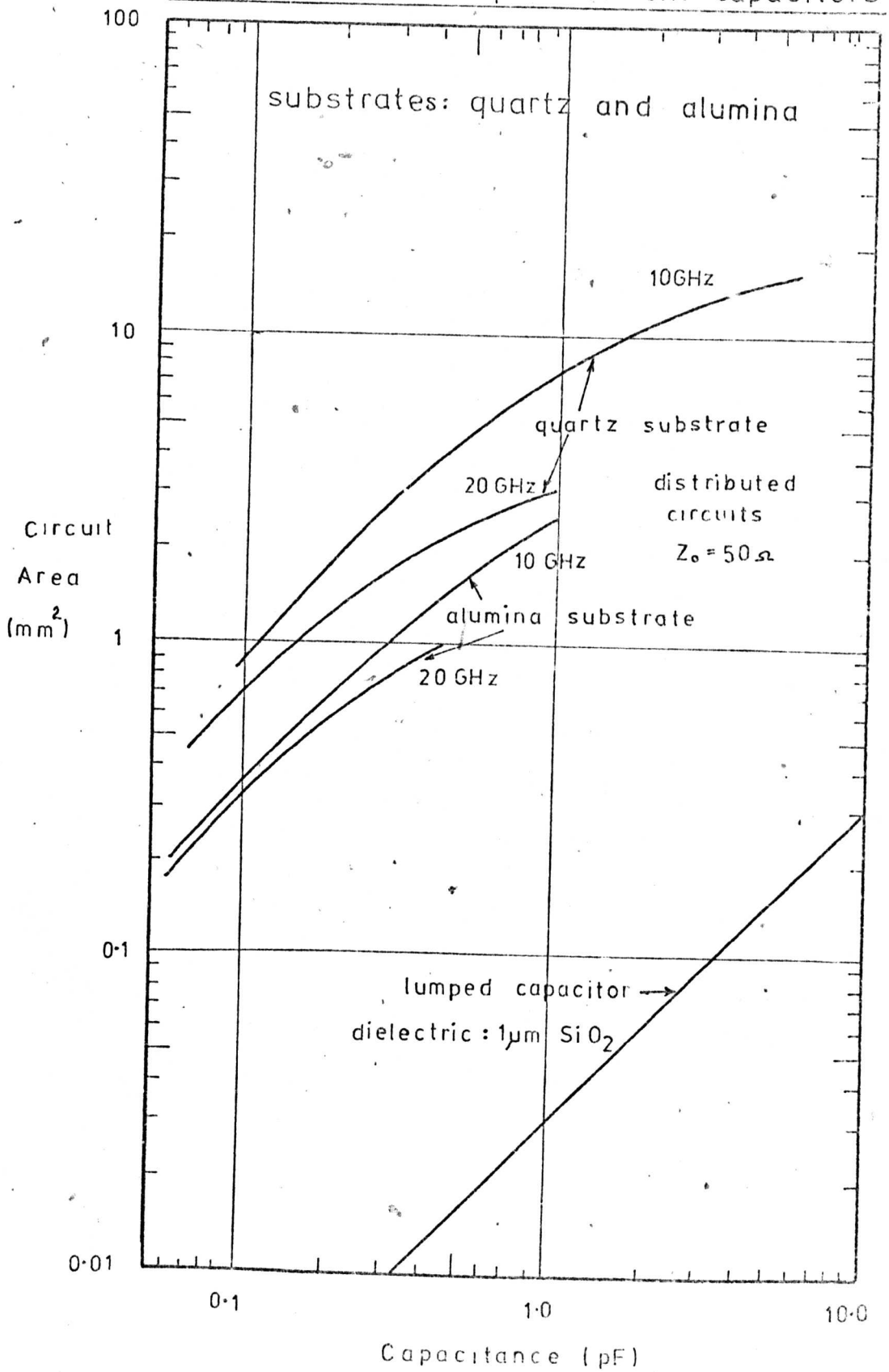
	Coax./waveguide	Microstrip	Thick film	Lumped element
size and weight	3	2	2	1
cost	4	3	1	2
reproducibility	3	1	3	2
reliability	3	1	1	1
circuit losses	1	2	3	3

Figure 1.3 Comparison of MIC techniques [8]

(in descending order of importance)

Figure 1·4

Comparison of substrate areas required for distributed and lumped-element capacitors



where Δf_{DE} is the distributed circuit bandwidth
Δf_{LE} is the L.E. bandwidth
C is the L.E. capacitance
Z_o is the microstrip line impedance
ω is the frequency

The resulting variation of $\frac{\Delta f_{DE}}{\Delta f_{LE}}$ with ωC is shown in figure 1.5. As discussed previously (sect.1.1) a practical lower limit for overlay capacitors is 1pF. Therefore at 10GHz, $\omega C \geqslant 0.06$. From figure 1.5 it can readily be observed that under these circumstances, for example, for a 50Ω microstrip line, the bandwidth of the L.E. circuit is approximately $2\frac{1}{2}$ times that of the corresponding distributed circuit.

3. the elimination of the distributed effects, and the introduction of conventional low frequency design techniques simplifies design procedures and thereby reduces production costs.
4. the elimination of conventional p.c.b. assembly techniques decreases the possibility of human error in fabrication and also decreases the number of mechanical-type interconnections. It therefore results in an increase in circuit reliability.

The major disadvantages are;

1. due to the smaller component size, the amount of energy stored by the device is considerably reduced compared with other forms of microwave circuits. i.e. the Q factor is considerably lower.
2. L.E. overlay capacitors require more processing stages, and therefore require more complicated manufacturing techniques, than their distributed counterparts. Also, due to the small size of L.E's, the quality of the photographic masks required to produce the components is significantly higher, resulting in larger setting-up costs and a slower turn-around time, but it is hoped that this will be compensated for by the step-and-repeat production.

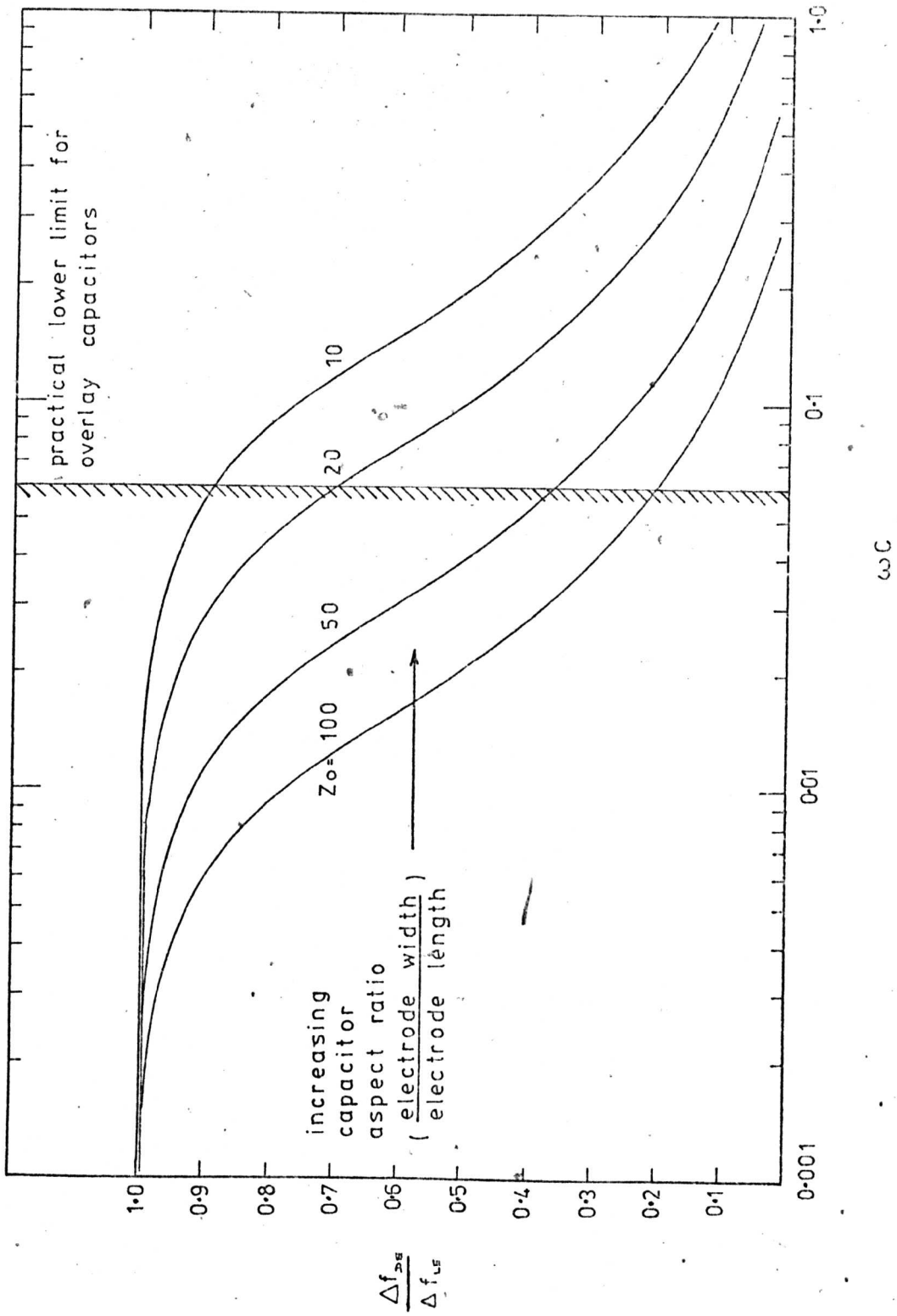


Figure 1·5 Comparison of the bandwidth of a distributed capacitor (Δf_{DS}) and a L.E. capacitor (Δf_{LE}) as a function of the capacitance C.

In conclusion, therefore, the advantages of L.E's are reduced size and weight, increased reliability, increased bandwidth and reduced cost, and the major disadvantages are those of low Q factor, the higher resolution required for the processing technique, and the slower turn-around time.

1.4 Integration of L.E's with active devices.

Two main techniques have been the subject of general investigation in the past as a means of integrating L.E's with active devices.

These are;

1. hybrid techniques[9], where semiconductor chips are bonded to ceramic, glass or sapphire substrates on which the passive L.E. devices are deposited.
2. monolithic techniques[9-11] where high resistivity ($>1{,}000\ \Omega$cm.) semiconductor wafers are used as the substrate material, and the L.E's are deposited directly on to the semiconductor wafer. Epitaxial layers are then grown for the active devices. Unlike low-frequency monolithic circuits, the isolation is resistive, as conventional p-n junction isolation in low resistivity wafers is not suitable due to excessive losses and insufficient isolation at microwave frequencies.[8]

Hybrid M.I.C's have the advantage that the substrates have high Q factors and are very stable with temperature variations, and a wide variety of device types can be used in the same circuit without difficulty. The bonding of the active devices eliminates component-package parasitics, but may introduce other parasitics between the circuit elements and the substrate.[1]

The semiconductor substrates required for monolithic techniques are generally unstable due to the presence of mobile carriers, and the substrate properties vary significantly during processing and circuit performance. In the past[11] monolithic techniques have used silicon substrates, but its widespread application at microwave frequencies has been restricted by the very low Q factors obtainable.

Since the packaging density of M.I.C's is relatively low, it is not apparent that the monolithic approach will offer any cost advantage over hybrid techniques in M.I.C's. Furthermore, since in monolithic circuits the devices are grown-in, only top-contact devices may be used. In addition, up to the present time, processing difficulties, low yields and poor performance have seriously limited the application of the monolithic technology to M.I.C's.

For these reasons, the hybrid technology is used almost exclusively, at present, in the 1 - 15 GHz region, and for the purposes of this thesis, hybrid techniques alone will be considered.

With the recent taming of gallium arsenide technology[12] however, the advantages this material offers as a substrate compared to silicon, and the additional factor that in the mm. wavelength band especially, monolithic techniques reduce the parasitic inductance between the circuit and the elements, there is every indication that monolithic techniques may prove to be extremely important in the future.

1.5 Selection of materials for hybrid M.I.C's.

To optimise the performance of L.E's, the materials used in their manufacture must be carefully selected. This section investigates the requirements for the substrate, conductor and dielectric materials, with a view to optimising the circuit performance of overlay capacitors in hybrid M.I.C's.

1.5.1 Substrate selection.

The sole function of the substrate is to provide a mechanical support for the circuit. Ideally, no microwave energy should propagate in the substrate, and therefore it should contribute nothing to the circuit losses.

The desirable features for a substrate for this application are;

1. the surface should have a centre-line-average (C.L.A.) of not greater than 0.05 μm.

Due to the small dimensions of the L.E. comp-

onents, a high circuit resolution is required (250 lines/mm. - Section 1.6), and this can only be reliably achieved with a substrate with a very high degree of surface finish.

In addition, the substrate should be free from surface voids and inclusions which are comparable in size to the resolution required.

To ensure high resolution during the photo-lithographical processing, the substrate should also be flat to within 1 thou[13].

It has been shown[14] (Appendix 1.2), that the overlay capacitor is very sensitive to structural variations in the substrate, and that the surface roughness has an exceptional effect on the circuit yield, the dielectric leakage and the capacitor life. ~~time~~. Further, the degree of surface roughness is known to be a major contributing factor to the density of pinholes in the dielectric layer[15].

It is also a well published fact that there is a definite correlation between the resistivity of conducting films and the degree of surface roughness[16]. For example, if the ratio of skin depth to r.m.s. surface roughness of a thin conducting film, is unity, then the increase in surface resistivity is approximately 30% [17].

Therefore, in the interests of high manufacturing yields, component quality and reliability, and high Q factors, a substrate with a low surface roughness is essential for hybrid M.I.C's using L.E. components.

2. the substrate loss ($\tan\delta$) must be less than 0.005 at microwave frequencies.

The attenuation of a microstrip line due to the presence of the substrate (α_d) (assuming a plane wave exists in the dielectric) is [18]

$$\alpha_d \doteq \tfrac{1}{2} \frac{\omega}{v_p} \tan\delta \quad \text{nepers/metre} \qquad 1.2$$

where v_p is the phase velocity.

Therefore, to reduce microstrip losses, the substrate tanδ must be kept to a low value. For most practical microwave substrate materials, the substrate losses are of the order of 100 times smaller than the microstrip conductor losses (Appendix 1.3).

3. as the L.E's must be small compared to a wavelength, the dielectric constant should be relatively low. A reduction in e_r increases the permitted L.E. size, thereby reducing conductor losses and increasing the Q factor possible. A decrease in the dielectric constant also means a smaller relative tolerance on the line widths can be achieved, with improved component tolerances resulting. A convenient range of values for the dielectric constant is $3 < e_r < 10$.
4. there should be no substrate deformation during processing, and the substrate should be chemically and physically compatible with the deposited film, so that it can withstand the materials and processes to be encountered.
5. the substrate should have a high dielectric strength and a high thermal conductivity.
6. it should have a high purity and constant thickness, and should be free from alkali ions, which may adversely affect the circuit performance on exposure to moisture[13].
7. the substrate should have a low cost.
8. the substrate should allow good adherence of conductors.
9. the temperature coefficient of expansion of the substrate should be compatible with the conductors used in the circuit to avoid loss of adhesion during processing, so that wide temperature specifications can be achieved.
10. the substrate should be amenable to sawing and cutting after processing.

Suitability of substrate materials.

Some of the most common substrate materials, with their more important properties, are listed in figure 1.6. The semiconductor materials have been included in this figure

Figure 1·6 Substrate material properties

DIELECTRIC MATERIAL	COMPOSITION	Dielectric Constant Er	Dielectric Loss at 10 GHz (tan δ)	Surface Roughness μm r.m.s.	$\frac{\lambda}{100}$ at 10GHz for 50 ohm microstrip line (μm)	Dielectric Strength KV/cm	Thermal Conductivity cal/cm²/cm/sec/W/°C	Linear Coefficient of expansion per °C from 20°C	Cost relative to Corning 7059	Comments
Corning 7059	Barium alumino silicate (alkali-free glass)	5·8	0·004 → 0·01	Optically smooth ∠0·005	147	50	0·01	$5·2\times10^{-6}$	1	Wavy 1-2 μm r.m.s.
Corning 7940	Fused silica (99·5% + of SiO_2)	3·78	0·00002	0·005	171	50	0·0032	$0·56\times10^{-6}$	10	No surface detail visible on S.E.M.
Quartz	SiO_2	3·78	0·0005	Optically flat and smooth ∠0·005	171	50	0·0032	$0·56\times10^{-6}$	10	〃
Sapphire +	Single crystal alpha alumina (100% Al_2O_3)	9·3 → 11·7	0·0006	〃	108 → 121	480	0·4	$5·0\times10^{-6}$	90	〃
Alumina (as-fired)	99·5% Al_2O_3 (manufact., M.R.C.)	9·6	0·00025	0·1	121	550	0·09	$6·3\times10^{-6}$	30	2 μm voids. grain size ∠ 1 μm
Alumina (glazed)	Coors ADS-96F	9·2	0·0004	∠0·025	121	500	0·003	$5·9\times10^{-6}$	30	very wavy with pits.
Silicon	2,000 Ω cm.	12	0·0075 *	Optically flat and smooth ∠0·005	107					
Silicon	10,000 Ω cm.	12	0·0015 *	〃	107					
Gallium Arsenide	10^7 Ω cm.	13·5	0·0000013 *	〃	102					
Amorphous Rutile		100	0·0004	〃	42		0·02			

\+ measurements taken perpendicular to the C axis

* calculated from $\tan\delta = \frac{\sigma}{\omega\varepsilon}$

for comparison purposes only, and as discussed in section 1.4, will not be considered as suitable substrate materials for the purposes of this project.

A thorough investigation of the other substrate materials has been made by Mehmet[19]. He has made measurements at microwave frequencies of the dielectric constant and tanδ using cavity techniques, while Butlin[7] has considered the substrate surface finish by visual investigation using a scanning electron microscope (s.e.m.), and by surface finish measurements using a Taylor Hobson 'Talysurf'. The results of some of Butlin's work will be used at a later stage in the project.

The ceramic materials have been found to be completely unsuitable for L.E's on the grounds of surface roughness, and due to surface ripples which are similar in size to the components being produced. Although the properties vary greatly from one manufacturer to the next[20], the surface finish is generally limited by the grain size (typically ≥ 1 μm) and the existence of large voids and holes.

Figure 1.7 shows an s.e.m. photograph of a typical surface of as-fired alumina (96.5% Al_2O_3).

Polishing of ceramic substrates does not produce completely satisfactory results because of pulled-out grains causing pits, which for polished Coors ADS-995 were up to 2 μm in depth. Polishing does, however, reduce the basic waviness but cannot, of course, improve the microstructure. High density alumina, when polished, shows a higher per centage of smooth area, and a lower incidence of pits which are much shallower than for less pure samples.[14]

Glazed alumina[21] has an optically smooth surface and therefore eliminates the surface roughness difficulties, but on the macroscopic scale, the substrate is extremely wavy and has a build-up of glaze towards the edge of the substrate. It is therefore impossible to achieve the high degree of resolution required for L.E's. The glaze also introduces inconsistencies in the dielectric constant across the substrate area, which is undesirable.

Sapphire overcomes the principal problem of surface roughness associated with the majority of ceramics, and in terms of the more important physical and electrical properties,

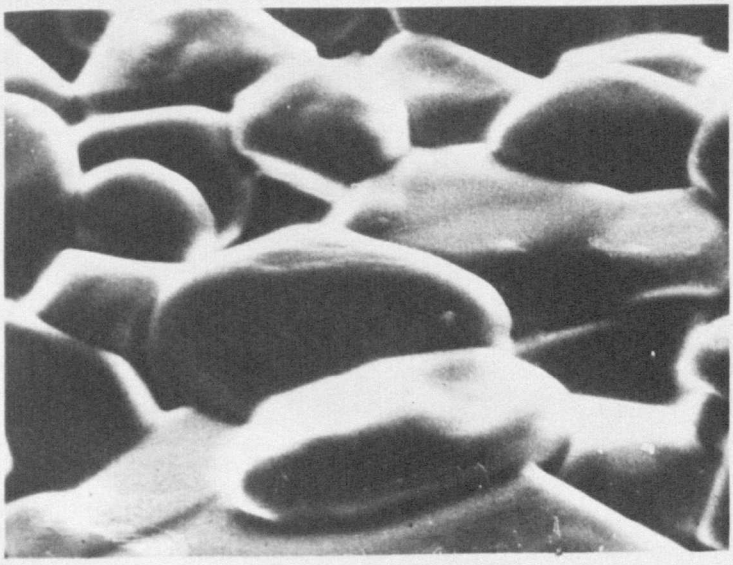


Figure 1·7 SEM photograph of the surface of an as-fired alumina (96·5%) substrate

is ideal as a substrate for M.I.C's. The cost is, however, substantial, and as far as L.E's are concerned, the dielectric constant is slightly high, which would result in increased demands from the processing technique, together with an increase in the component conductor losses.

The glass-based substrates can be produced with excellent surface finish, but a disadvantage of these materials, compared with ceramics, is their relative lack of physical strength.

Corning 7059 has a surface finish and dielectric constant ideal for L.E. components, but the microwave loss is relatively high. The substrates are, however, cheap, and have been used substantially in this project for the initial development of M.I.C. processing techniques, particularly because of the excellent surface finish properties.

Fused silica (quartz, Corning 7940) has a very smooth surface when polished, a low dissipation factor and a low dielectric constant, which is accurately known and does not vary from batch to batch. It is also comparatively cheap. It has good workability, resulting in a uniform thickness over a large area, is easily cleaned and easy to metallise. It is however, brittle and easily cracked.

Considering the advantages it offers over other available materials, quartz was selected as the most suitable substrate material for this project, and for relatively cheap hybrid M.I.C's in general. The particular substrates used were 066 quality silica, supplied by Gooch and Housego, Ltd..

Substrate thickness.

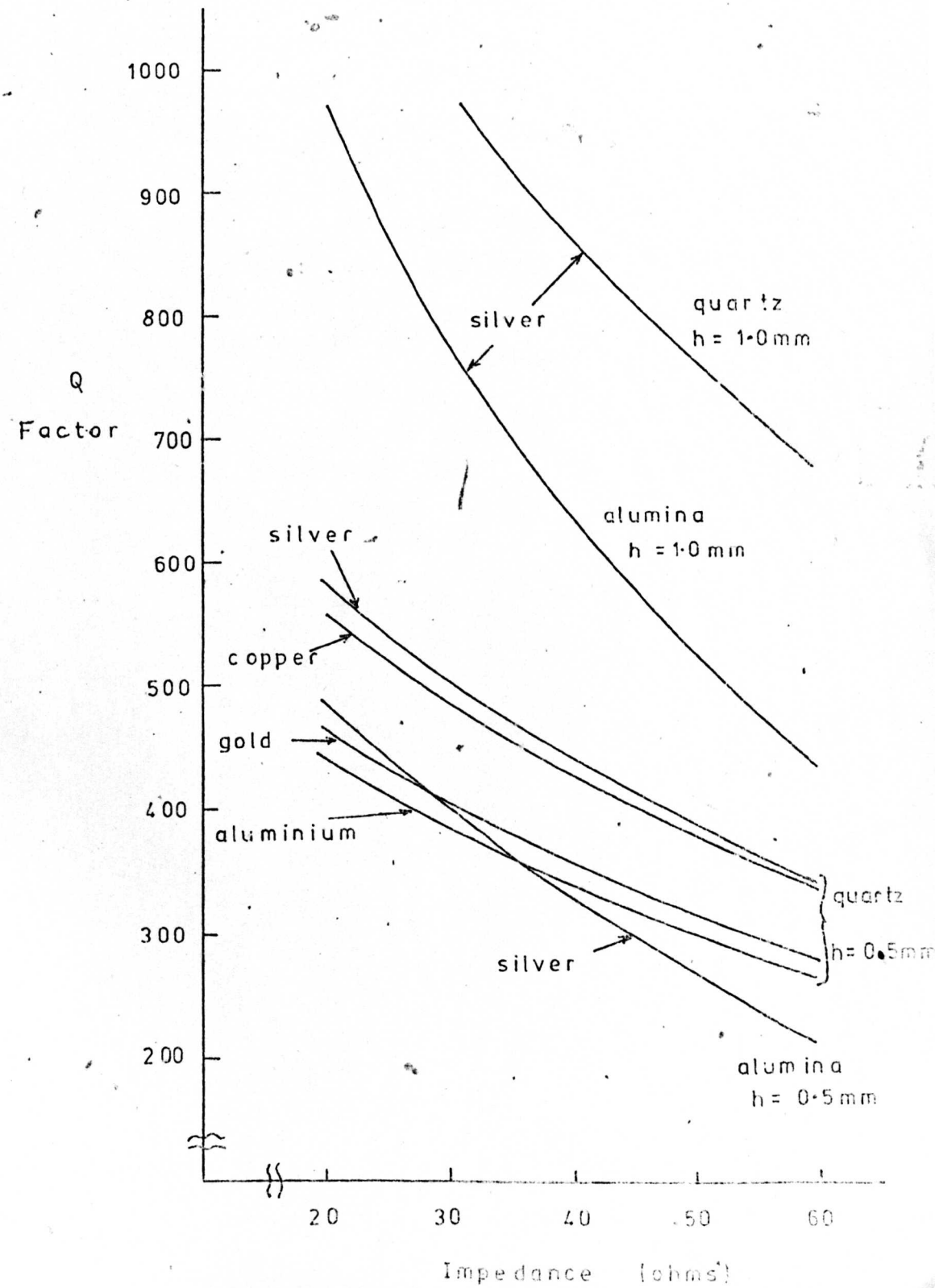
The thickness of the substrate does not directly influence the properties of L.E. capacitors, but it does have a direct effect on the Q factors of the microstrip interconnections. This is demonstrated in figure 1.8, which shows that the Q factor is virtually directly proportional to the substrate thickness, h.

While the Q values can be increased by using thicker substrates, this tends to increase the overall circuit size and the thermal resistance[9], and if the thickness of the

Figure 1·8

Microstrip Q factor as a function of characteristic impedance at 10GHz

(Appendix 1·3)



substrate exceeds $\frac{\lambda_o}{4\epsilon_r}$ [8], higher order surface modes, and modes with longitudinal field components can be excited. This tends to increase the losses and introduce excessive coupling to other parts of the circuit. For quartz substrates at 10 GHz, the thickness should therefore be less than 2mm..

A substrate thickness which gave sufficiently high microstrip Q factors ($\doteq$400), yet gave amenable dimensions for practical microstrip lines, (a line width of 1mm. for a 50Ω line), was 0.5mm., which was chosen as the standard thickness for the quartz substrates used in this project.

1.5.2 Conductor selection.

The main requirement for conductors for M.I.C's is to present the minimum resistance to current flow. To ensure this, the metal conductivity must be high, the surface roughness low, and thickness of the deposit a minimum of 2 skin depths.[18] Also, due to the high current density, the quality of the longitudinal edges of the conducting strips is very important, and a square cross-section improves the conductivity by up to a factor of 2.[22]

The highest Q factors in the past have been obtained using evaporated thin films[23] which are then electroplated to the required thickness. This method produces higher Q factors than for thick film techniques[16,24,25] which offer significant processing simplifications.

Thick film methods[26] are however impractical for this application as the resolution required for L.E's at 10 GHz is 250 lines/mm. (sect. 1.6) and the resolution attainable by thick film techniques is 5-10 lines/mm.[27]

The Q factors of evaporated films are comparable to those of electroplated films[28] and, therefore, an alternative approach for producing the conductors is to evaporate the required thickness and then to define the conductors by etching. However, etching the relatively thick layers ($>1.5\mu m$) results in loss of edge acuity, with subsequent reduction in Q factor and a reduction in component tolerances.

The preferred technique for defining the conductors is therefore to evaporate a thin film ($\doteq$ 0.25μm) of the material, and then to electroplate to the required thickness.

Having selected the deposition method, the material choice to optimise component performance remains to be determined.

The basic requirements for thin film conductors for M.I.C's are;

1. the material should have a high conductivity.
2. the surface of the conductor should be smooth.
3. there should be good adhesion to the substrate.
4. there should be compatibility with other materials in the circuit.
5. the material should be resistant to oxidation and tarnishing.
6. the material should have a low temperature coefficient of resistance.
7. the material should be easy to solder to, and easy to etch.
8. the coefficient of expansion of the conductor material and dielectric material used in the capacitor, must be similar and diffusion limited, if heat treatment is to be used. Also, compatability with other materials is important if stress during bonding of active devices, is to be avoided.

Material selection.

The properties of some of the more important conductor materials are given in figure 1.9.

The microwave conductivities of thin films, and of plated films, are lower than the bulk material values[7,28], and to a large extent, accurate values are untabulated. At the outset of the project, therefore, a comparison of possible conductor materials could only be made using the bulk material properties.

Figure 1.8 shows the improvements in microstrip Q factor possible by a suitable choice of conductor material. It can be seen that the theoretical Q factors attainable with silver and copper conductors, are approximately 20% higher than those possible with gold. As the major contributing factor to microstrip loss at microwave frequencies is conductor loss (Appendix 1.3), this difference is considered to be extremely significant.

Material	Conductivity[9] $10^{+7}\ \Omega^{-1}\ m^{-1}$	Coefficient[4] of linear expansion[3] $\times 10^{4}$	Skin depth[9] at 10 GHz μm	Adherence[2] to dielectrics	Comments on Au or Cr
Copper	5·8	0·18	0·66	very poor	little resistance to corrosion
Gold	4·09	0·15	0·79	very poor	
Silver	6·17	0·21	0·642	poor	little resistance to corrosion
Aluminium	3·72	0·26	0·825	very good	cannot be plated
Chromium	0·77	0·09	1·81	very good	

Figure 1·9 Conductor material properties

Unfortunately, both silver and copper are both subject to tarnishing and oxidation, and if they are to be used, extreme care must be taken during the processing to avoid damage to the films, and the completed circuit must be protected with a thin layer of gold.

Silver was investigated initially because of its high conductivity, but was discarded at an early stage due to processing difficulties (section 2.4.11).

Processing of copper films was found to require a certain degree of care due to the problems of tarnishing, particularly during the processing stages. It also has the disadvantage of being readily attacked by most etchants.

Gold was found to be very simple to process and has the advantage of being amenable to bonding, which is an important requirement for hybrid circuits. It has the disadvantage, however, of having a lower conductivity than copper, which makes it slightly less desirable in certain applications (Chapter 7).

Aluminium has the disadvantage that it cannot be electroplated. As the required thickness of the conductors is to be achieved by plating methods, aluminium is clearly unsuitable.

In the light of these factors, it was decided that where it is warranted by high conductivity requirements, copper would be used as the conductor material, protected, as necessary, by a very thin layer of gold. However, where the requirements of conductivity are not so demanding, and ease of processing is more important, the emphasis would be placed on the use of gold as the main conductor material.

Seed layer.

As indicated in figure 1.9, the adhesion between both gold and copper films, and the substrate, is very poor. It is a well-adopted practice to introduce a "seed" layer between the metal film and the substrate to improve adhesion. Ideally, the seed layer should be a very highly resistive material, which has good adhesion to both metals and dielectrics. Such a material is chromium.

In order to achieve the desired adhesion, the seed layer should be at least 100 Å thick[24], but to ensure that the microstrip loss is not increased at 10 GHz, the seed layer should be less than 500 Å [8]. In practice, a 200 Å layer of chromium was used as the seed layer in all microstrip circuits discussed in this thesis.

1.5.3 Capacitor dielectric selection.

The requirements for a material to be used as a dielectric in microwave capacitors are;

1. there should be a very low incidence of pinholes.
2. the dielectric should have a low dielectric loss.
3. the dielectric should have a reproducible dielectric constant.
4. the voltage breakdown should be relatively high (> 200 volts).
5. the dielectric should display a high stability.
6. amorphous films are required for isotropic properties, and a good surface finish.

Material selection.

Figure 1.10 shows the most important properties of some common microwave dielectric materials.

The material most commonly used, due to the ease of deposition, is silicon oxide, but the properties of the final deposit depend significantly on the deposition technique.

If evaporation techniques are used, the high temperature involved allows dissociation (loss of O_2). The final composition of the dielectric is affected, very sensitively, by the evaporation conditions, and studies of evaporated silicon oxide show that it is amorphous and loosely packed, and varies in composition from SiO to SiO_2[29].

Electron beam evaporated silicon oxide appears denser than the thermally evaporated deposit[29].

Both electron beam and thermal evaporation techniques have the advantage of relatively high deposition rates.

Sputtering of silicon oxide allows more control over the composition of the dielectric due to the lower temperature

MATERIAL	METHOD OF DEPOSITION	RELATIVE PERMITTIVITY	DISSIPATION FACTOR Units AT 1 kHz	BREAKDOWN STRENGTH kV / cm
Silicon oxide	Evaporation	2 → 4	0·01 → 0·04	100
Silicon oxide	Sputtering in oxygen — argon	3·4	0·005	3,000
Silicon oxide	Deposition from silane	3·8	0·002	10,000
Alumina	Electron beam evaporation	8·8	0·008	4,500
Tantalum oxide	Sputtered in oxygen — argon	25	0·01	700
Tantalum oxide	Sputtered in argon and anodised	25	0·008	6,000

Figure 1·10 Dielectric material properties

of the process, and also results in higher Q values than is possible from evaporated films. The density of pinholes is also significantly reduced. However, it is a slow deposition method and does not lend itself to covering cross-overs and surface discontinuities as well as other techniques (namely the deposition from silane).

The deposition of silicon oxide from silane produces the highest purity deposit, with the highest oxygen content, and after densification, it has the lowest loss compared with films deposited by other techniques. The technique has the advantage that the SiO_2 grows normal to a hot material surface, and therefore the density of pinholes, especially at cross-overs, is significantly reduced, which is an important advantage for capacitor applications.

Adsorbed moisture from the atmosphere can play a very large part in the observed dielectric losses of silicon oxide, and it is normal to densify the dielectric after deposition, by baking at 750-1000°C to drive off the water[30].

Silicon oxide was chosen as one of the dielectric materials for investigation, due to the ease of processing, and the abundance of published data on its low frequency performance.

The deposition technique adopted was r.f. sputtering, which appears to produce results only slightly inferior to silane deposition methods, which were not available for this investigation.

Aluminium oxide was also briefly investigated as a dielectric material to provide a comparison with silicon dioxide.

1.6 Requirements for the processing techniques for L.E's.

Before components can be designed and fabricated, acceptable component tolerances must be determined so that suitable processing techniques, to the required standard, can be developed. Further, since the microwave L.E's can rarely be tuned, the component tolerances must be kept to a bare minimum.

If, for example, for a 1pF capacitor, using 1μm of

SiO_2 as dielectric, a tolerance of ± 5% is required, then the width, or length, of the capacitor must be controlled to within at least ± 2.5% (or approximately ± 4 μm for a capacitor aspect ratio of 1, neglecting dielectric thickness variations). In terms of quality of the fabrication process, therefore, we require a resolution of at least 250 lines/mm to achieve the desired performance.

The other factor contributing to the tolerance of the capacitor is the dielectric thickness, which, for this example, must be controlled to within a maximum variation of ± 5% (i.e. ± 0.05 μm for this application, neglecting electrode dimension variations).

The corresponding tolerance for microstrip lines is not so stringent. A tolerance of ± 1% for a 50 ohm microstrip line using an 0.5mm thick quartz substrate requires a width tolerance of ± 2% (i.e. ± 20μm) or a resolution of 50 lines/mm..

The corresponding tolerance for the substrate thickness is ± 1.8% (i.e. ± 9 μm).

The particular substrates selected for this project were nominally 0.020" thick, and had a measured variation across the substrate of, on average, ± 0.3%. The variation in absolute thickness of 27 samples taken from several different production batches, was ± 2.5%, which would result in a variation in microstrip line impedance of ± 1.4%, or 0.7 ohms in 50, if the nominal substrate thickness was assumed. This would probably be satisfactory for the majority of normal microstrip circuits, but in view of the stringent demands required for the capacitor measurement technique, it is considered unsatisfactory in this application. The thickness of each substrate is therefore measured prior to processing, using a Tesamaster direct-reading micrometer, which has a measurement accuracy of ± 0.75 μm.

1.7 Conclusions.

The conclusions of this chapter, in brief are;

1. the L.E's are approximately 1/100 of the size of the corresponding distributed elements.

2. the L.E. Q factors will be lower than the corresponding distributed element Q factors.
3. the L.E. circuit bandwidth will be equal to, or greater than the bandwidth of the corresponding distributed circuit.
4. hybrid integration techniques will be adopted for the investigation in this thesis.
5. the substrates to be used are 1"x1"x0.020" fused quartz (e_r=3.78).
6. the conductor deposition technique will involve deposition of a thin film (0.25μm) of the material by evaporation, then subsequent electroplating to the required thickness of at least 1.5μm to reduce the microwave losses.
7. copper and gold conductors will be used for the electrodes and interconnections.
8. the capacitor dielectric will be deposited by r.f. sputtering.
9. the dielectric material to be studied in greatest detail will be silicon oxide, although some comparison will be made with aluminium oxide.
10. the processing techniques to be adopted must have a resolution of at least 250 lines/mm..

2. BASIC THIN FILM PROCESSING TECHNIQUES

2.1 Introduction.

In chapter 1, the basic aims of the project were outlined (namely the fabrication and measurement of thin film overlay capacitors), and some of the features required of the processing techniques to reliably attain these aims were discussed. However, the methods finally adopted to satisfy the requirements are, to a certain extent, governed by the processing facilities available. This chapter explains briefly the equipment available and the processing techniques adopted, and indicates the extent to which the author was involved in their development.

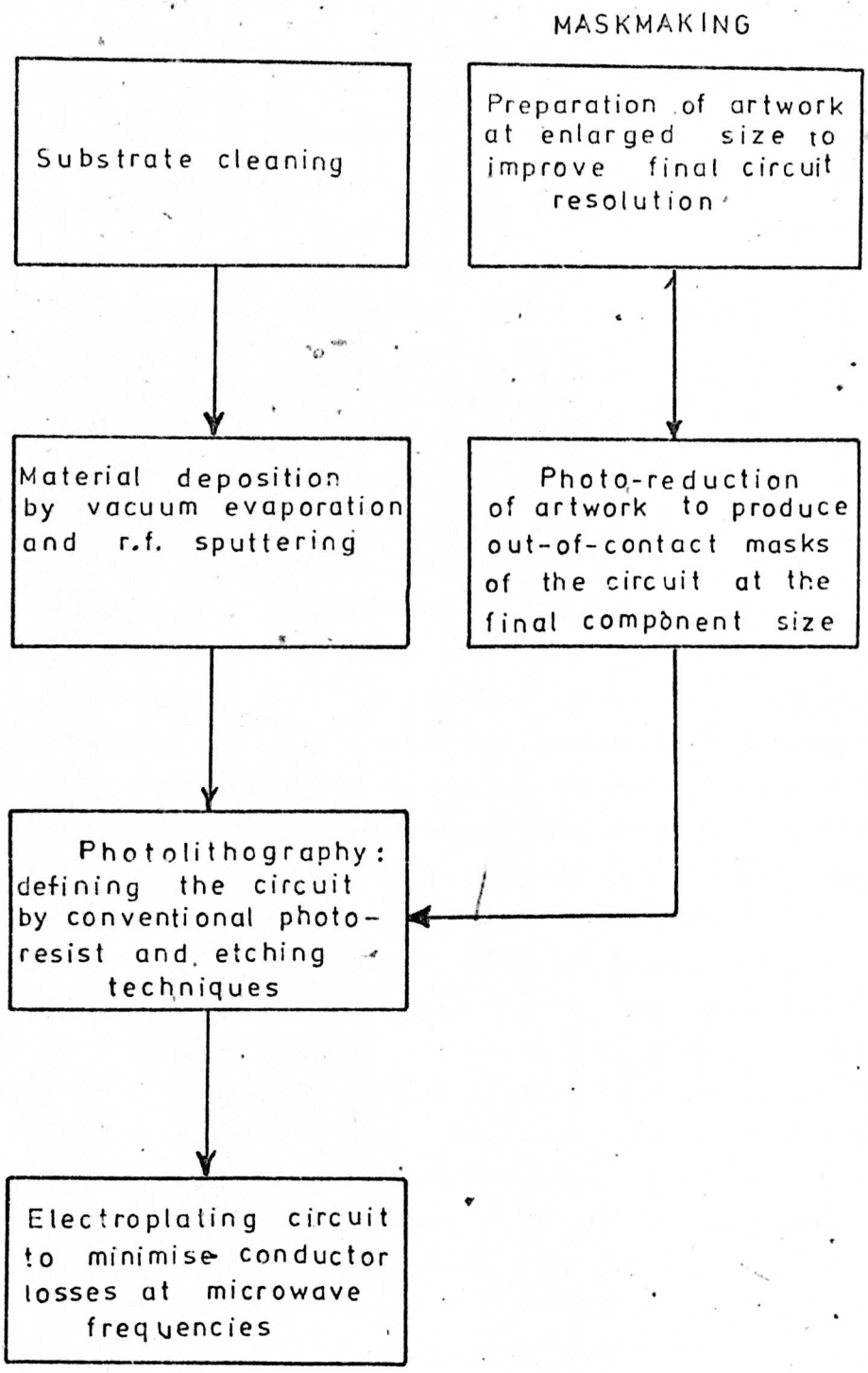
Although a considerable amount of time was invested in developing equipment and optimising techniques, it is not considered relevant to discuss all these details here. Relevant references will therefore be made at the appropriate places, and only the most significant experiments will be discussed in detail. In particular, the effects of glow-cleaning on film adhesion, the effect of resist post-baking time on undercutting, and the effect of copper etchant, and its application, on the undercutting of copper films are described.

2.2 General thin film techniques.

The basic techniques[24] adopted for producing M.I.C's, which were determined in chapter 1 are (figure 2.1);

1. the deposition of conducting and insulating layers by vacuum evaporation and r.f. sputtering.
2. the definition of components and circuits using out-of-contact masks, and conventional photolithographical techniques.
3. the electroplating of the conductors to a thickness of several skin depths to reduce microwave losses.

The equipment available, and the processing techniques adopted for each stage in the process will now be discussed



Basic Processing Procedure

Figure 2-1

in detail, but techniques peculiar to the fabrication of a particular component will be discussed in the appropriate chapter.

2.3 Maskmaking.

2.3.1 Preparation of the artwork.

The master artwork, from which the photographic mask is produced, is prepared[31] on Keuffel and Esser Cut'N Strip film, using a Coradi Coordinatograph (KDB-161).

The coordinatograph has cutting facilities in the X and Y directions and has a useful cutting area of 400 mm x 450 mm.. With extreme care, lines can be positioned to an accuracy of ± 0.02mm, and a single cut in the film can be less than 10 μm in width.

The artwork is then photographically reduced in a Class 10,000* clean room. The room temperature is maintained constant to within ± 2°F by means of a recirculating-air-conditioning unit. The air is filtered to 0.4 μm at 99.98% efficiency, and maintained at a slightly positive pressure to exclude dust particles. There are 12 air changes per hour.

The clean room water supplies are filtered to 1 μm, and all processes are performed under safety light conditions. Operators are completely embalmed in protective clothing to minimise particle contamination of the room, and the walls are p.v.c. lined to reduce dust generation.

2.3.2 The reduction camera.

The camera (figure 2.2) is a single stage variable reduction system from which reductions of between 5 : 1 and 80 : 1 are available. The artwork is illuminated from the rear, which allows a contrast ratio of up to 1000 : 1, compared to a possible 40 : 1 for front illumination[33].

With extreme care, two consecutive reductions are possible over a very small working area (less than 5mm image

* For a Class 10,000 clean room, the particle count per cubic foot has not to exceed 10,000 of 0.5 μm or larger, and 700 of 5 μm or larger [32].

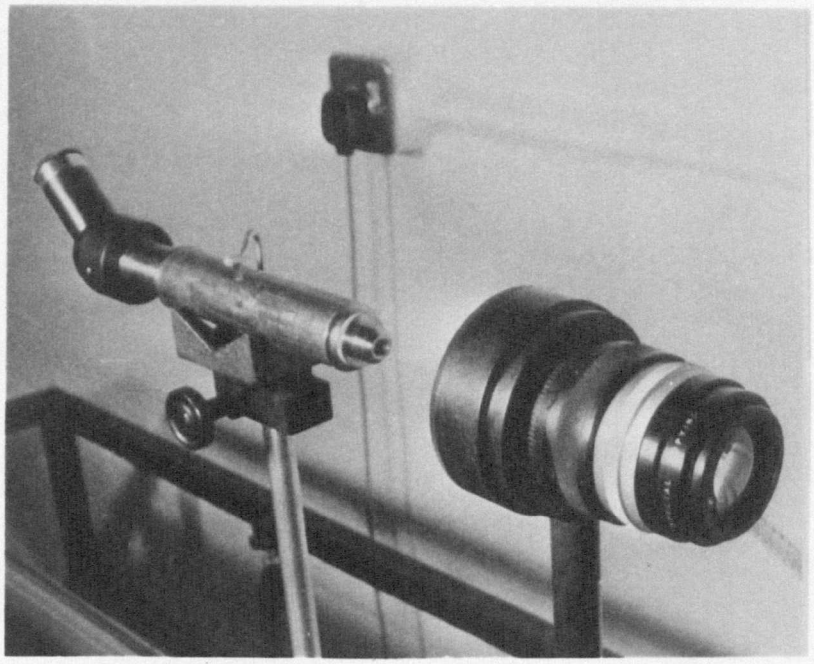
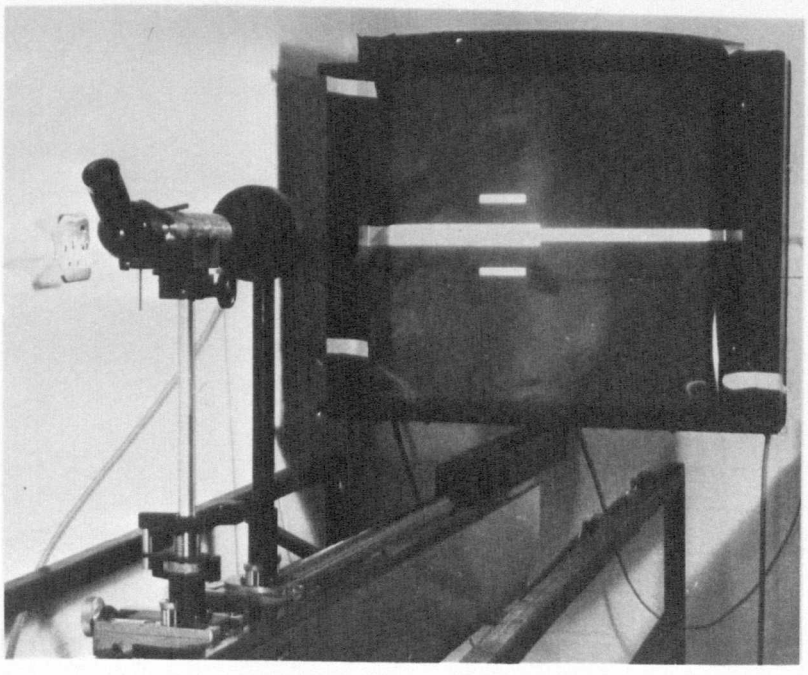


Figure 2·2 Camera and focussing microscope

Figure 2·3 Camera and artwork holder



diameter), and reductions of 250:1 have been achieved.

The camera and light-box are both mounted on a calibrated optical bench, 230 cms long (figure 2.3), suspended by springs from a heavy steel base, which provides a vibration-free support.

Variable reductions are achieved by moving the camera position relative to the artwork holder on the optical bench, and calibration charts of optical-bench scale setting versus reduction, and bench position versus lens focus setting, have been experimentally obtained[31] for each of the three lenses in use.

These lenses are;

1. Kern Paillard 26 mm Bolex lens.
2. Rank Wray special copying lens, 10:1 reduction.
3. Rank Wray special copying lens, 25:1 reduction.

The main specification details of the lenses are given in figure 2.4.

The camera can be positioned on the optical bench to within $\pm$ 0.025mm. This positioning error has negligible effect on the accuracy of the reduction and focus calibration charts due to the depth of field and focus of the lenses[35].

The photographic plates used are Kodak 2"x 2" High Resolution plates because of their high resolving power (2000 lines/mm)[37], their high acutance, and their fine grain.

The light source consists of 8x 20 watt green (λ = 530 nm.) fluorescent tubes to ensure high contrast ratios[36], and the exposure time is controlled by means of an electronic timer switching the lights, hence no shutter vibration is transferred to the camera. The intensity of the tubes is regularly monitored by use of a light meter to assess when replacement is necessary.

The maximum image size available for a given lens at a given reduction is shown in figure 2.5.

As stated previously, the majority of processing is carried out using 1"x 1" substrates, and therefore, from figure 2.5, it can be seen that the maximum practical reduction which will result in the exposed area of the mask covering the complete substrate area, is approximately

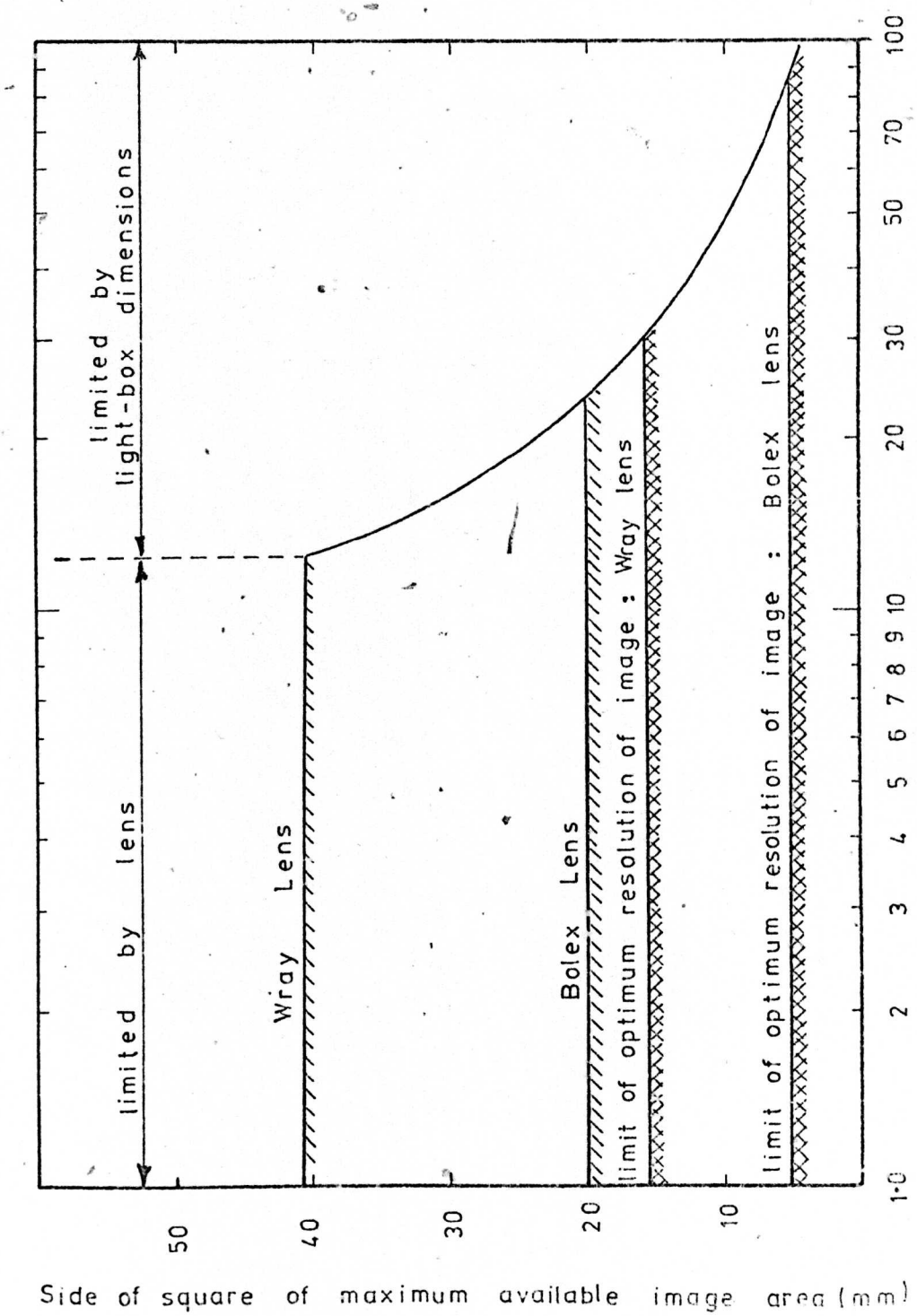
	LENS		
	Bolex	Wray 10:1	Wray 25:1
Focal length (mm)	26·0	77·3	77·3
Reductions available	5:1 → 80:1	5:1 → 25:1	5:1 → 25:1
Optimum reduction	—	10:1	25:1
Apertures available	f/1·9 → f/22	f/4 → f/16	f/4 → f/16
Resolution at maximum aperture (μm)[34]	1·23	2·59	2·59
Resolution at maximum aperture (lines/mm)	814	397	397
Depth of focus at maximum aperture (μm)[35]	4·84	40·8	40·8
Recommended maximum useable area of image (ref. 36) diameter of circle (mm)	4·34	12·9	12·9

Details of Photographic Lenses

Figure 2·4

Figure 2·5

Image size v Reduction

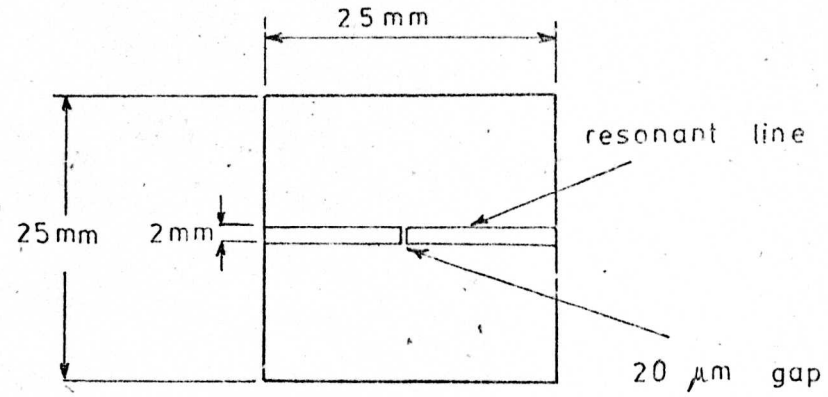


17.5 : 1 using the Wray lenses. At this reduction, the ± 0.02 mm tolerance on the artwork means that to produce a strip with a tolerance of ± 2.5%, which has been shown to be a practical requirement for M.I.C's (sect. 1.6), then the minimum strip width possible is 45.7 μm. As will be observed later, this is larger than some of the microstrip gaps required. Therefore, in these cases, the masks must be made using larger reductions, but over a smaller working area, using the Bolex lens. This then introduces the need for additional masks to allow alignment of the high resolution masks to the correct position on the substrate. For example, the masks (and the artwork from which they originate), required to produce the circuit of figure 2.6 (a), (a resonant line with a 20 μm gap in the centre), are shown in figures 2.6 (b) - (g). Had it been possible to achieve the desired resolution and cover the required substrate area at the same time, the circuit could have been made with only one mask. The final image quality however, is improved by using the additional masks, as a larger aperture (lower f number) can be used on the Bolex lens, thereby increasing the resolution (figure 2.4) and increasing the contrast[38] (figure 2.7).

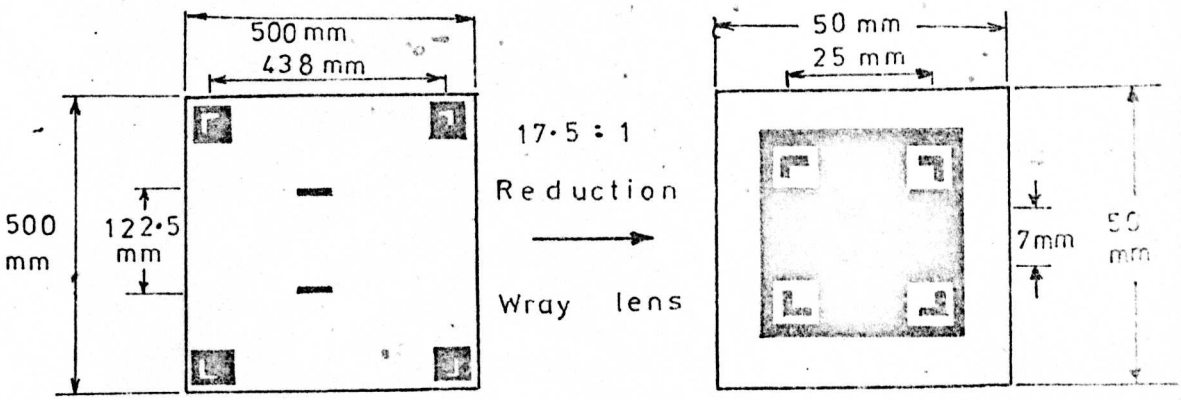
This limitation also means that to permit accurate alignment of masks produced at different reduction factors, probably using different lenses, the reductions of each of the lenses must be known to a high degree of accuracy, (typically better than ± 0.5%).

To achieve this latter requirement, considerable effort has been expended in optimising the reduction, focus and exposure procedure. This was initially carried out by Kelland[39] who commissioned the camera, and in particular the Bolex lens. Subsequently, after camera modifications to improve the photographic system, the optimisation was repeated by the author for both the Bolex and the Wray lenses. The commissioning procedure, and the operating instructions, together with the relevant references, are well documented[31,39] and will not, therefore, be repeated at this stage.

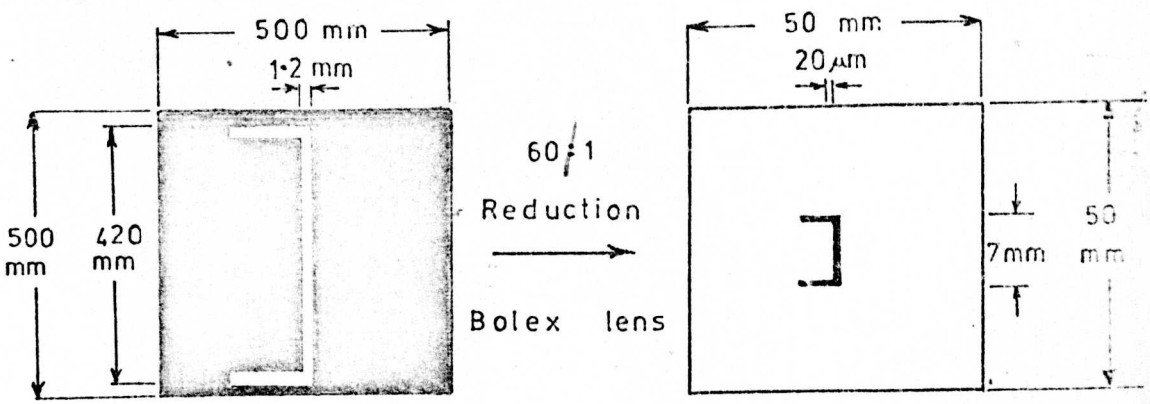
Qualitative evaluation of the masks was made using an Olympus Metallurgical Microscope of x 1000 magnification, using transmitted light, and a micrometer eyepiece, capable



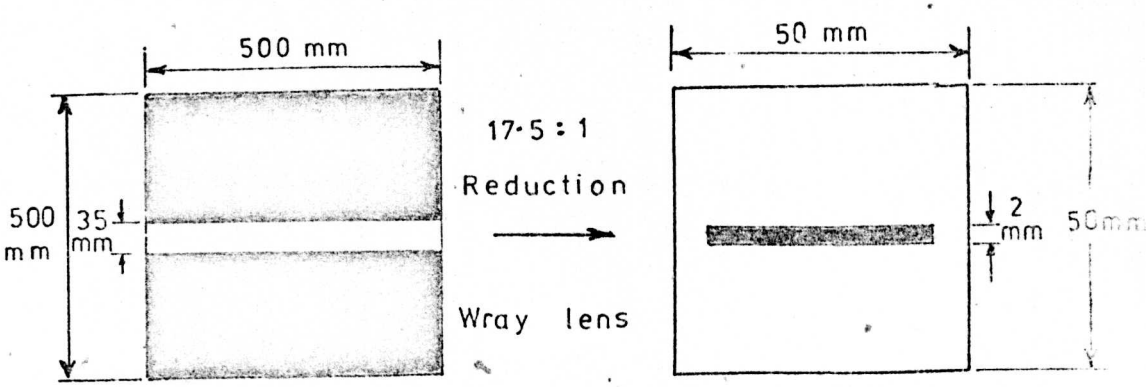
(a) Microstrip Circuit



(b) alignment line artwork (c) alignment line mask



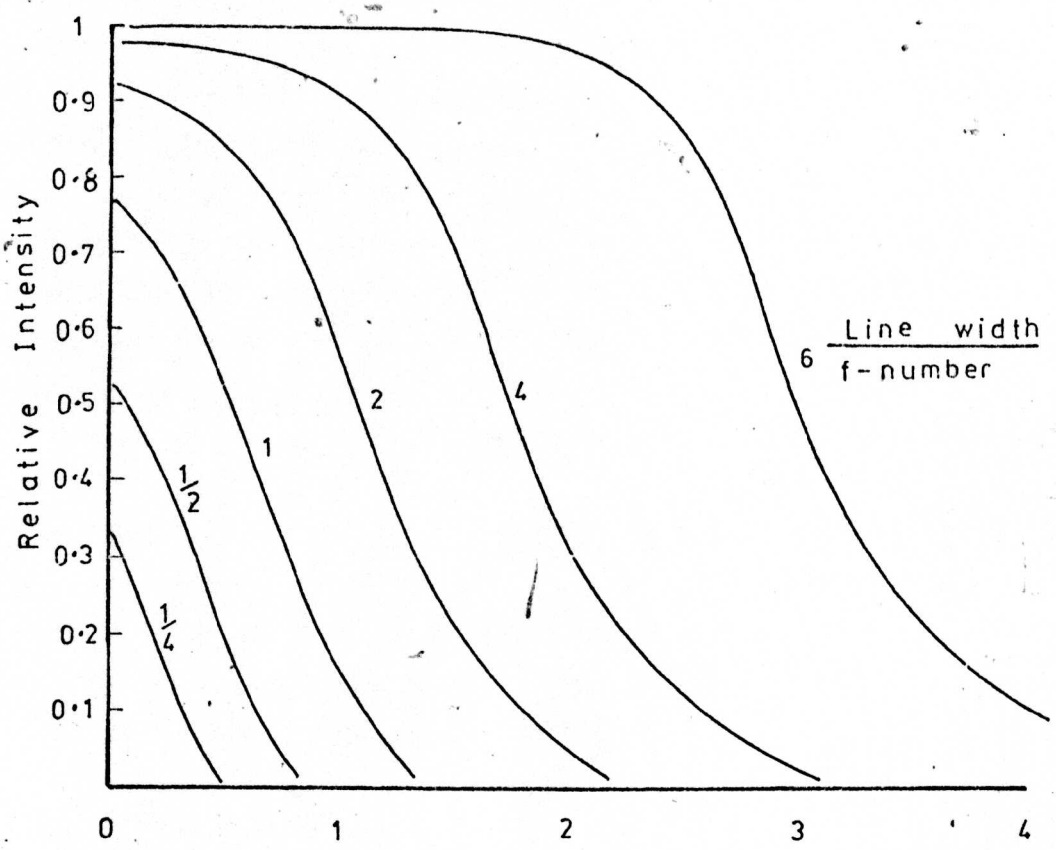
(d) gap artwork (e) gap mask



(f) Resonant line artwork (g) Resonant line mask

Microstrip circuit (a) with the masks (c,e,g) and artwork (b,d,f) required to produce it.

Figure 2·6



Effect of f – number on image intensity

Figure 2·7

of measuring to ± 0.05 μm. The original artwork was measured on a Leitz Projection microscope, which has a measurement accuracy of ± 0.005 mm..

2.3.3 Photographic processing.

The processing of the exposed plates (figure 2.8) is a standard process, commissioned by Kelland[39], which is applicable to all exposed plates. To minimise contamination of the masks, the chemicals are filtered to 0.5 μm prior to use. To ensure reproducibility, the processing is carried out using a semi-automatic processing unit, which guarantees reproducible agitation in each bath.

For the majority of applications, using an average contrast light source, it has been found that, providing the exposure times and the lens apertures used are as stated[31], the data obtained from the reduction and focus charts[31] is more than adequate for obtaining images of the required reduction, focus and contrast using the processing schedule of figure 2.8.

The narrowest line width so far achieved using the standard processing data is 2.6 μm, which is a higher resolution than the requirements of this project demand.

A more stringent set of processing stages is given in reference 40 should this be required.

2.4. Photolithography.

All photolithographical processing (i.e. metal and dielectric deposition, photoresist processing, etching and plating) is carried out in a Class 100,000 clean room, in which the temperature is maintained constant to within ± 2°F. The air is maintained at a slightly positive pressure to exclude dust particles, and is filtered to 0.4 μm at 97% efficiency. There are 8.6 air changes per hour.

2.4.1 Photolithographical facilities.

The photolithographical facilities available in the

Solution	DEVELOPER
Time	4 minutes
Preparation	1 pt. Kodak DG 10 to 6 pts. water

↓

Solution	STOP BATH
Time	1 minute
Preparation	3 pts. glacial acetic acid to 8 pts. water

↓

Solution	WATER RINSE
Time	2 minutes

↓

Solution	FIXER
Time	8 minutes
Preparation	130 gms Kodak Unifix to 1 litre water

↓

Solution	WATER RINSE
Time	2 minutes

↓

Solution	HYPO – CLEAR
Time	10 minutes
Preparation	30 gms Kodak Hypo-clear to 1 litre water

↓

Solution	WATER RINSE
Time	10 minutes

↓

Solution	ISO – PROPYL ALCOHOL
Time	2 minutes

↓

Dry by standing the substrate in a clean atmosphere in a vertical position for 5 minutes

Processing of Photographic Masks

Figure 2·8

clean room are;

1 Birvac electron-beam coating unit, with facilities for evaporation from multiple sources. The substrate support has been modified (figure 2.9) to accommodate 2 x one inch square substrates, which can be rotated to coat the two large faces, and two edges of the substrate during one evaporation run. This facility greatly reduces processing time for fabricating microstrip lines with short circuits. The thickness of the deposit is monitored by an Edwards thin-film thickness monitor which registers the change in resonant frequency of a quartz crystal in the vacuum chamber, as the crystal mass changes due to the depositing material.

2. R.F. sputtering unit[7], for the deposition of dielectric materials.

3. Two clean-air benches (figure 2.10) constructed by the author, in which the majority of photolitho - graphical processing is performed. The benches produce a constant flow of filtered air from the front of the units, thus preventing dust from entering. A predominant feature of the design, is that the substrates can be processed virtually entirely without being removed from the clean-air cabinets, due to the equipment being arranged in the correct processing sequence (i.e. substrate cleaning at the left-hand side of the left-hand bench, progressing in succession to final inspection at the right-hand side of the right-hand bench). A hatch is provided in each bench to allow transfer of substrates between benches without removal from the clean-air conditions.

The main features of the clean-air benches are;

1. ultrasonic tank, with a recirculating deionised water supply. The water is deionised (Appendix 2.1) in a single ion-exchange column (Elgastat B106) producing a resistivity of 10-12 Mohms. The same water supply, additionally filtered to 1.2μm

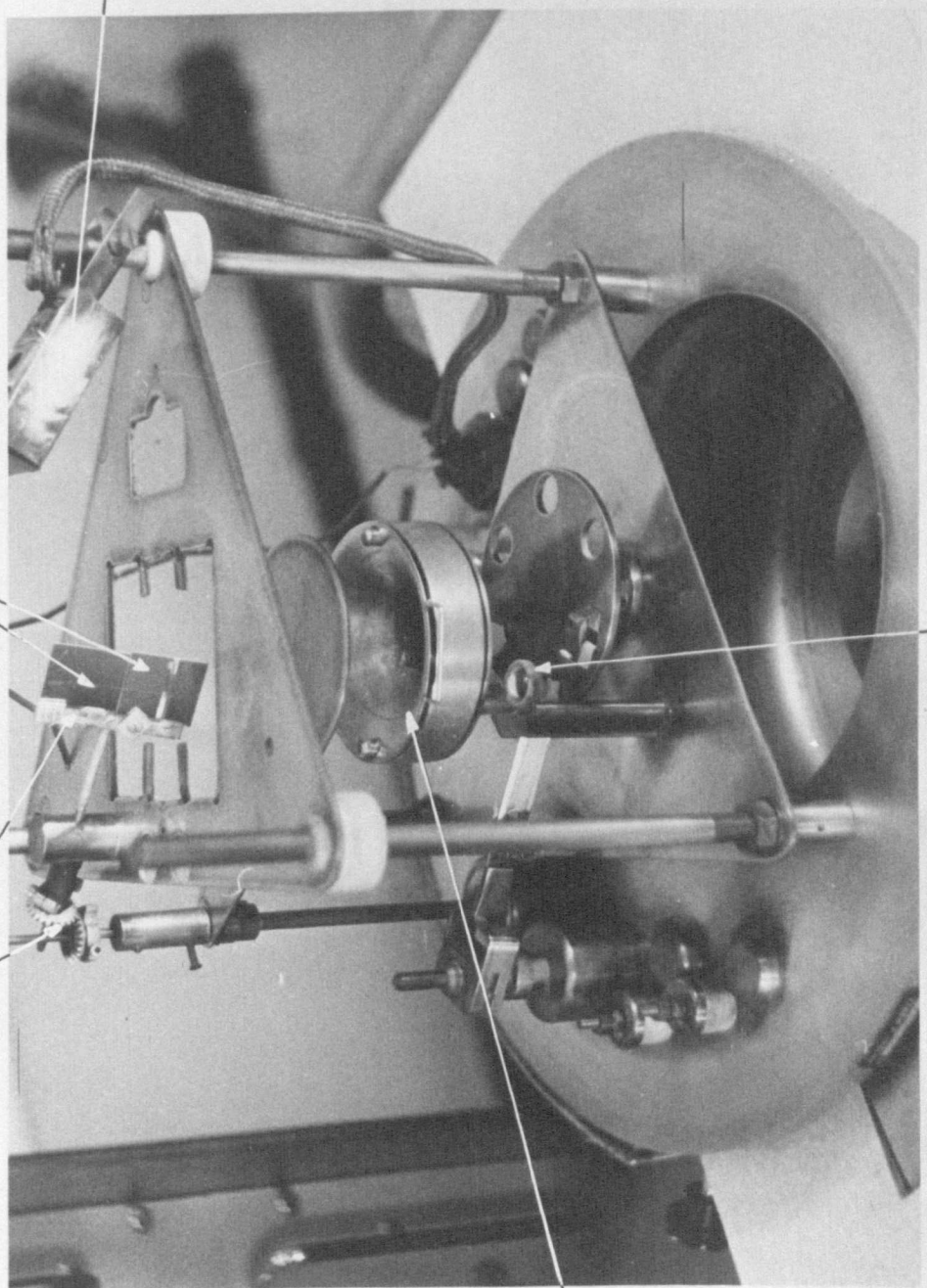


Figure 2-9 Evaporation unit

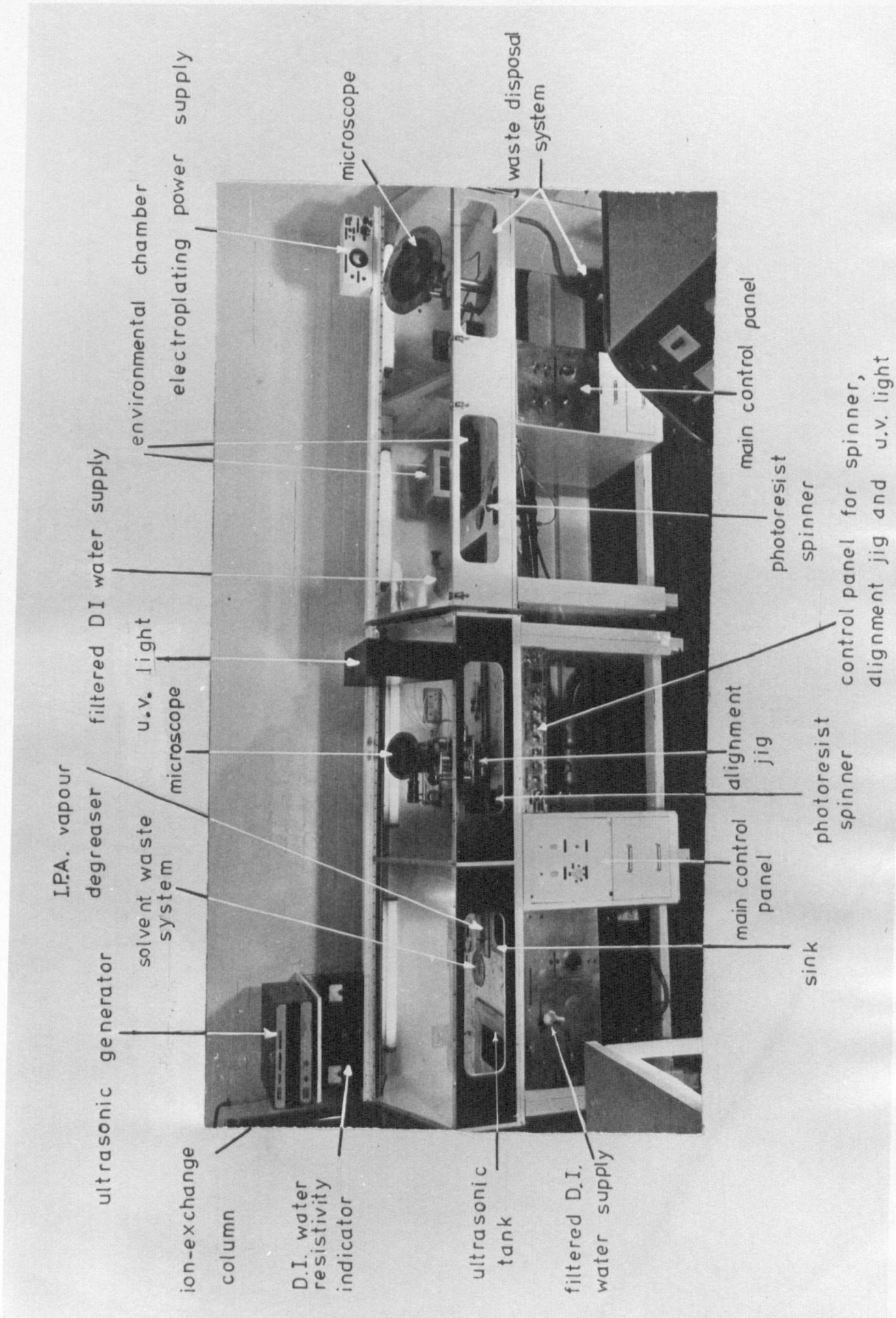


Figure 2·10 Clean-air Cabinets

by a Millipore filter, is available at two other tap outlets, one on each bench. The ultrasonic generator is a Dawe instrument, and operates at 25 kHz with a peak power output of 300 watts.

2. iso-propyl-alcohol (I.P.A.) vapour degreaser bath with thermostatic control for substrate and film cleaning.
3. two substrate spinners, for photoresist application and for spin-drying substrates. The substrates are held in position by vacuum supplied from a vacuum pump below the bench. The spinners are interlocked with the vacuum pump to prevent the spinner being operated before the pump is switched on.
4. mask alignment jig, for aligning 2" x 2" masks and 1" x 1" substrates.
5. photoresist exposure system for up to 1" x 1" substrates, incorporating a 500 watt water-cooled mercury vapour lamp (Philips SP500W) situated $12\frac{1}{2}$" from the substrate. The lamp power supply is interlocked with a water-flow switch to protect the lamp in the event of cooling-water failure. Exposure times of less than 1 minute are electronically controlled by operation of a shutter, and for longer exposures, a manual overide switch is incorporated.
6. environmental chamber with thermostatic control for photoresist drying and baking.
7. constant-current power supply (100mA maximum output) for electroplating up to 1" x 1" samples.
8. Olympus SZ zoom inspection microscope with x 1000 magnification.
9. disposal systems for liquid waste disposal.

2.4.2 Substrate preparation.

The key to high yields in any thin film processing unit is cleanliness, and this is of prime importance before the deposition of the initial layers of the circuit. It has

been shown[41], for example, that the initial substrate cleanliness has a great influence on the pinhole density of films.

The results of comparative tests of various cleaning techniques are described by Putner[42], and the cleaning cycle adopted (figure 2.11) is predominantly a standard process, based on Putner's findings.

For recycled substrates, the first stage is a standard trichloroethylene degreasing cycle. The metal remains of previous circuits are then thoroughly removed from the substrate by immersing in aqua regia (1 part conc. nitric acid to 3 parts conc. hydrochloric acid). New, unused, substrates, have an initial degreasing stage, but there is no requirement for the acid dip.

All substrates are then ultrasonerated in a 2% solution of Decon 75[43]. This detergent was found to be much more effective in its cleansing action than the more commonly used Teepol. Decon 75, however, should not be used with borosilicate glasses, which it attacks. The substrates are then thoroughly ultrasonerated in deionised and filtered water to remove the detergent. Thereafter, a standard solvent cleaning process is used. In this process, the thorough cleaning in acetone is to ensure that all the trichloroethylene has been removed, and the I.P.A. rinse is to ensure that the acetone is completely removed. Failure to do so will result in substrate staining in both cases. Following the cleaning process, the substrates should be transferred immediately to the vacuum chamber.

2.4.3 Vacuum evaporation.

Substrates requiring either one or two short circuits are mounted on the rotating substrate holder (figure 2.9), which is electrically and thermally floating. This allows the substrate to rise to its own temperature during the deposition, without forced cooling, resulting in excellent film adhesion.

To ensure a clean surface for deposition, the substrates are glow-cleaned (Appendix 2.2) during the diffusion pump cycle. This technique has the advantage over glow-cleaning during the rotary pump cycle, in that the evaporation

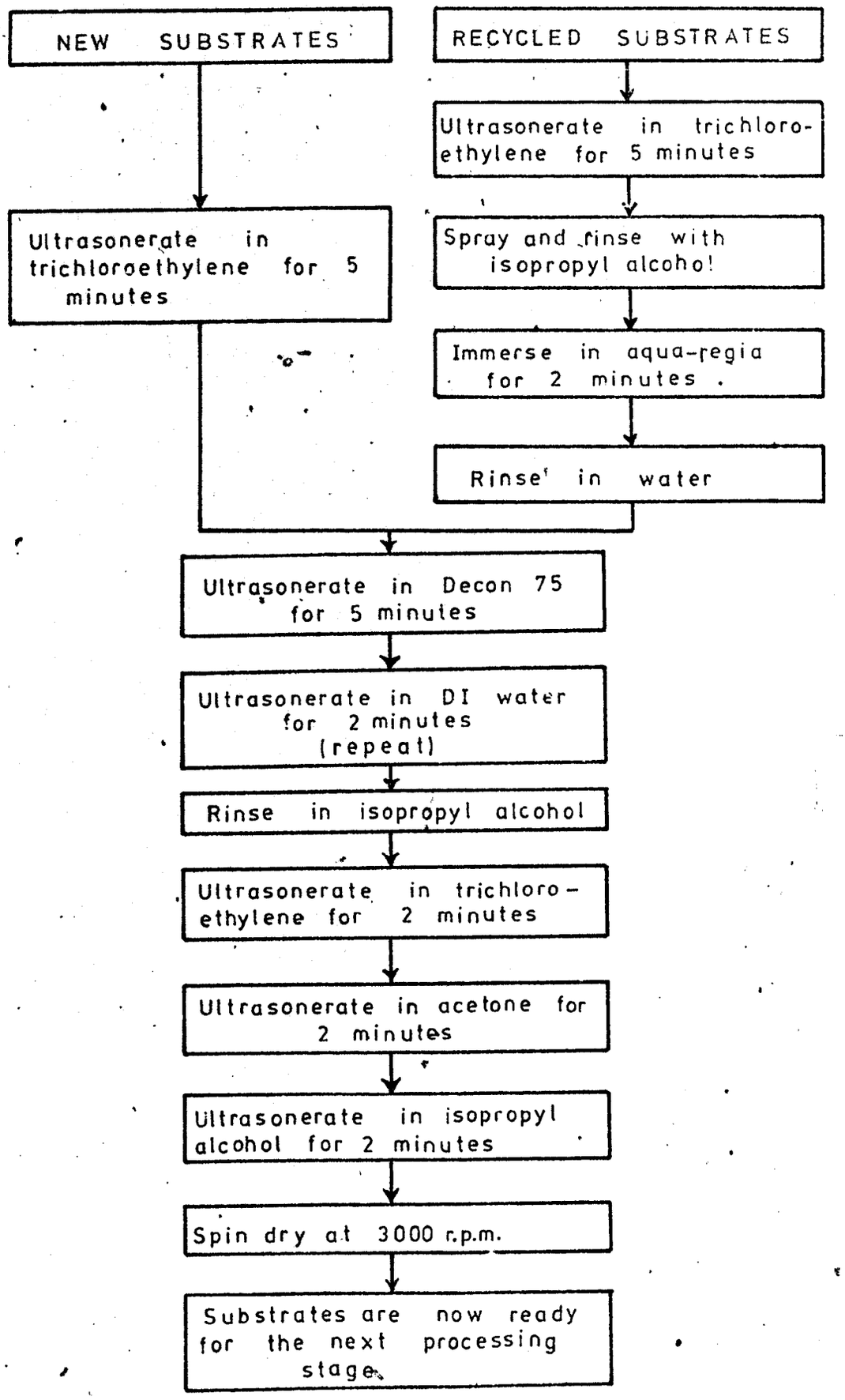


Figure 2·11 Substrate Preparation

can be carried out much sooner after the glow-cleaning stage, with resulting improved film adhesion[44].

After glow-cleaning, the bell jar pressure is then allowed to fall to approximately 1×10^{-5} Torr, and the evaporation is then commenced using the conditions described in Appendix 2.3.

For all applications, a 200 Å seed layer of chromium is deposited initially, to improve the adhesion of the main deposit. Then, without breaking the vacuum, and as quickly as possible, a layer of at least 2500 Å of the main metal is deposited. If the time lag between the evaporations is too long, then the chromium tends to oxidise with resulting loss in adhesion, as confirmed by others[45].

The vacuum system is then allowed to cool for at least 30 minutes before the substrates are removed from the bell jar, to prevent excessive oxidation of the films.

2.4.4. The effect of glow-cleaning on film adhesion.

Work by several people[46,47] has shown that glow-cleaning, under certain conditions, can be beneficial to film adhesion. Holland[46] has shown that coatings of oil may be absorbed on to the surface of the substrate due to the discharge warming the neck of the diffusion pump, and heating the oil. He also describes elaborate electrode systems which prevent the effect occurring. This effect can, however, be eliminated by using a nitrogen trap, or alternatively, by glow-cleaning during the rotary pump cycle. However, Bateson[44] has shown that after 30 minutes in a vacuum system, there is no difference between a sample which has been glow-cleaned and one which has not, and Stoddart[47] has shown that there is little difference between films aged in vacuum and air.

Best results are obtained[48,49] by glow-cleaning whilst bleeding air into the system and pumping with the diffusion pump, rather than glow-cleaning whilst pumping with the rotary pump alone (which would result in a longer time lag between the glow-cleaning stage and the deposition).

Due to the rather foreboding warnings of Holland[46] concerning the possible worsening effects of glow-cleaning,

and the requirement for elaborate electrode systems to ensure proper cleaning, it was decided to test the effectiveness of the Birvac unit for glow-cleaning purposes.

For the test, 36 samples (microscope slides, with C.L.A. of 0.007 μm) were cleaned using the cleaning cycle of figure 2.11. All samples were coated with 200 Å of chromium as a seed layer, and 0.5 μm of copper. One batch of 12 samples was coated without glow-cleaning (group A). One batch was glow-cleaned during the rotary pump cycle, and coated 30 minutes later (group B). The final batch of 12 was glow-cleaned during the diffusion pump cycle, whilst bleeding air into the system (group C), and coated 30 minutes later.

All samples were removed from the vacuum unit 30 minutes after coating, and the Scotch tape test[50-52] for adhesion applied. The results showed that only two samples of group A passed the test, indicating good adhesion on those samples, 12 samples of group B passed, and 12 samples of group C passed.

Therefore, even considering the general unsatisfactoriness of the Scotch tape test, there is considerable evidence to show that glow-cleaning improves the adhesion of vacuum deposited films.

2.4.5 R.F. sputtering.

A detailed description of the design and operation of the r.f. sputtering unit, which is used for the deposition of dielectric films, has been documented by Butlin[7], and will not, therefore, be repeated here.

The substrates to be sputtered are mounted on a water-cooled substrate support, and the lower substrate surfaces are coated with vacuum grease to aid heat dissipation. In this way, the substrates are maintained at approximately 25°C throughout the deposition run, which increases the deposition rate[53], without reducing the deposit quality.

The quality of the deposited film, generally improves with lower deposition rate[7], and these factors have been varied to a limited extent, in Chapter 9, for the microwave capacitor measurements. A suitable compromise between film

quality and processing time, for quartz and alumina films, is given by the deposition conditions stated in Appendix 2.3.

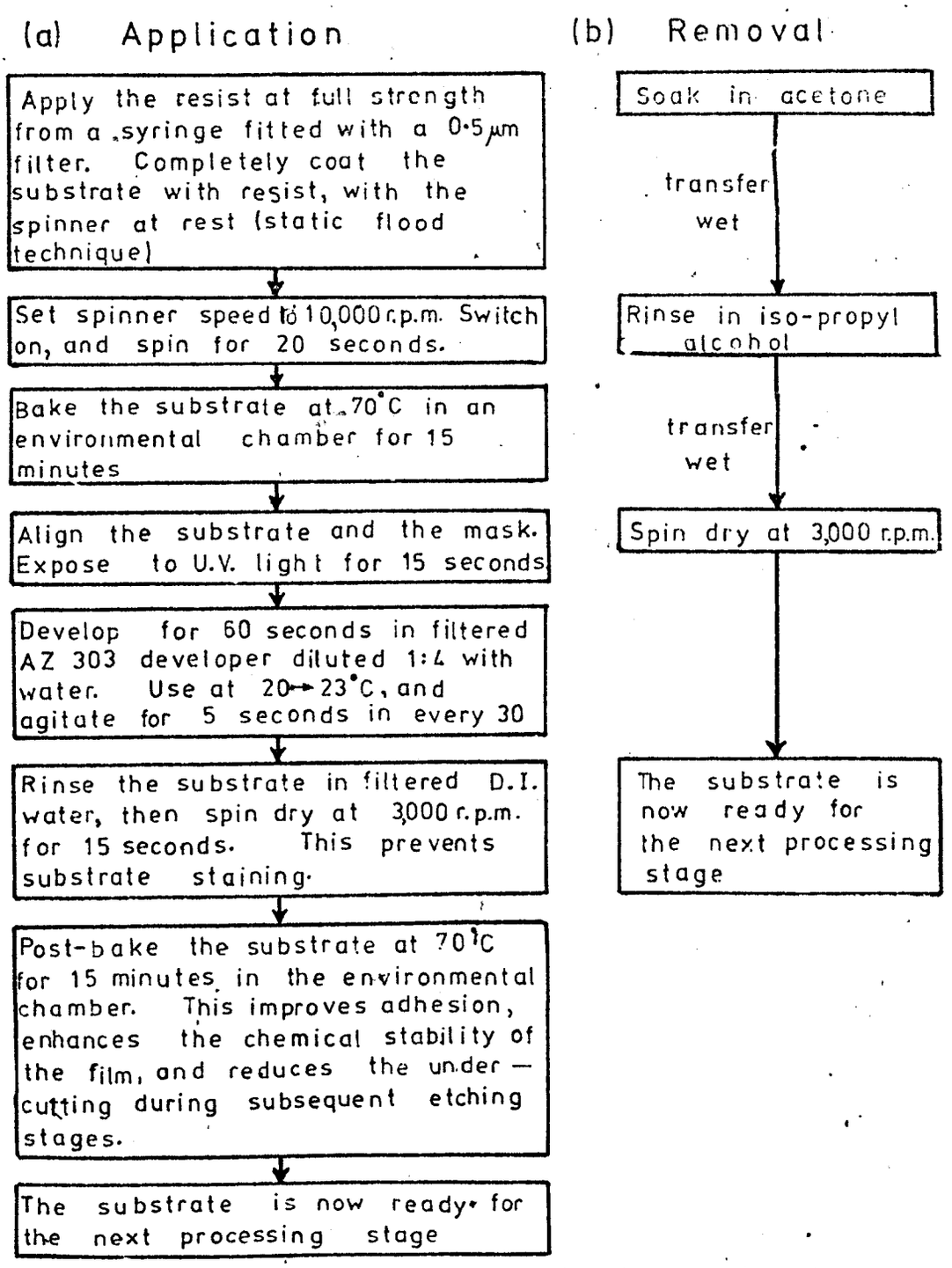
Once more, cleanliness is essential, and the dielectric target is sputtered for at least 15 minutes before deposition is commenced, to ensure removal of surface contaminants.

2.4.6. Positive photoresist processing.

All photoresist processing is carried out in the clean-air benches, which have gold fluorescent safe-lights, and gold perspex tops to reduce unwanted exposure of the resist by the clean-room lighting.

The complete process for the application of the positive resist (Shipley AZ 111) is summarised in figure 2.12. The most important features[54] are;

1. the resist should be filtered before application. This reduces the pinhole density by half compared with non-filtered resists, removes particulate matter and reduces the viscosity of the resist, thereby producing a resist coating of more uniform thickness[41].
2. the spinner thyristor speed-control circuit has been designed specifically to produce a uniform film of reproducible thickness. For a given resist, the thickness and uniformity of thickness, is determined by the spinner acceleration, the final speed, and the extent to which the final speed is constant[55]. In this case, the resist thickness (measured by multiple beam interferometry) is 0.6 μm (0.5 pinholes/mm^2)[41], and variations in thickness across a 1" x 1" quartz are less than 7%. The pinhole density was sufficiently small for the vast majority of applications.
3. the resist pre-bake must be carefully controlled, as too long, or too short a pre-bake will result in slowing of the emulsion speed, with resulting under-exposure of the resist. Too short a pre-bake also results in resist swelling during the development stage, with subsequent loss of resolution. The pre-



Application and removal of Shipley AZ 111 Positive Photo-resist

Figure 2·12

bake improves resist adhesion, drives off residual solvents, aids levelling and minimises dust inclusions[56]. The prebake, exposure and development times, have been carefully selected to improve dimensional control.

4. the developing time is critically dependent on the temperature of the developing solution, and it should be kept between 20 - 23°C. Too high a temperature will result in softening of the resist and loss of resolution[56].

The process for the removal of the resist is also given in figure 2.12. At this stage, with copper films, it is extremely important to keep the substrates wet at all times during the resist removal, otherwise the films will be stained by the acetone. These stains will prove difficult to remove without severe etching of the copper surface. On the other hand, it is very important to avoid prolonged washing as oxidation of the deposited films will result.

The spin-drying of the substrates was found to be the best method of drying without producing staining of the films, which is a problem encountered with slow-drying methods.

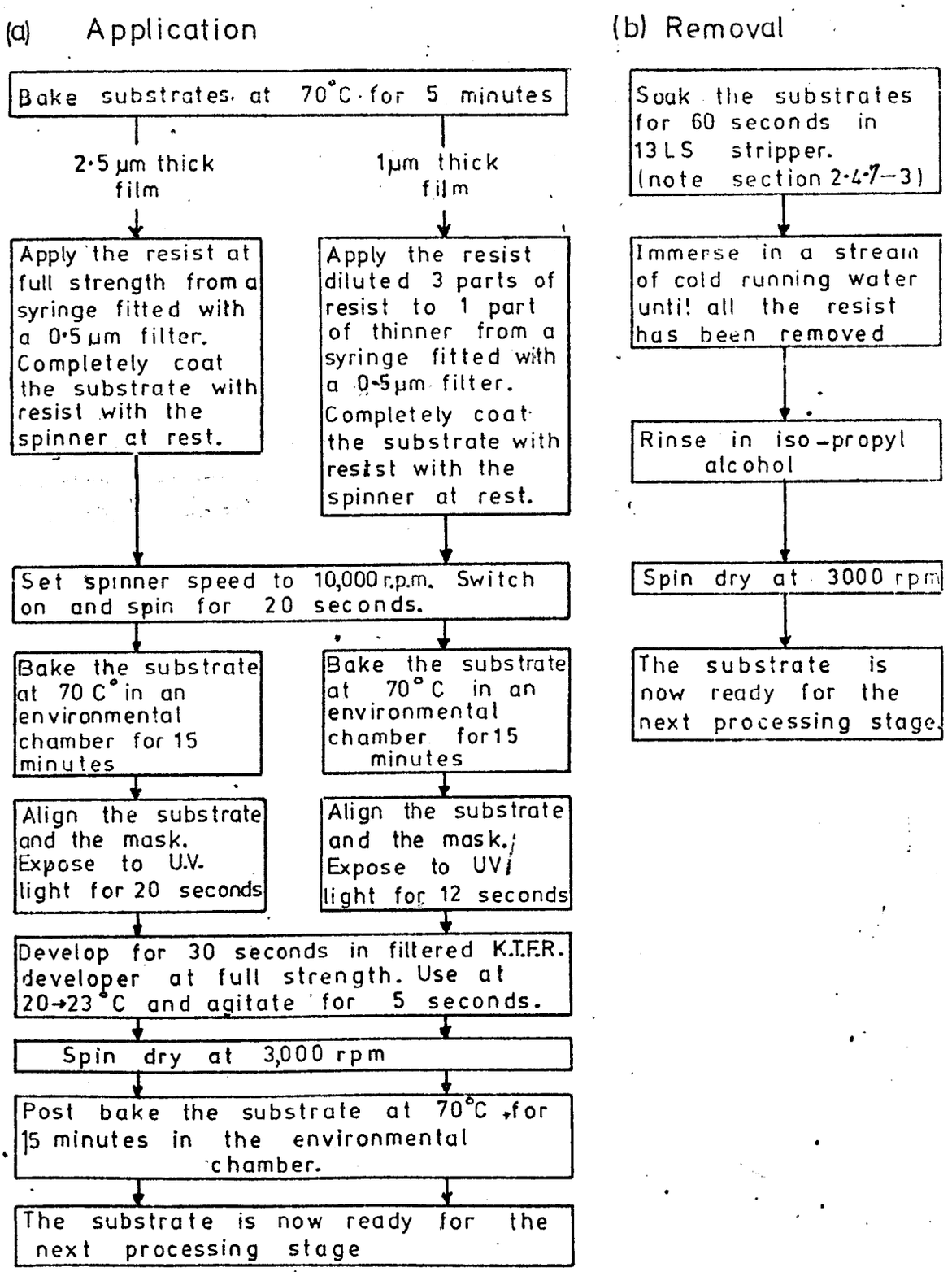
2.4.7. Negative photoresist processing.

The negative resist used in the thin film processing, is Kodak Thin Film Resist (K.T.F.R.)[54,55,57], which can be thinned as required with K.T.F.R. thinner. Unlike positive resist, whose resolution appears to be unrelated to the resist thickness, the resolution of K.T.F.R. improves with a decrease in resist thickness, and as a general guide, the thickness of the K.T.F.R. should be approximately $\frac{1}{3}$ of the width of the finest line[58].

Htoo[59] has shown that the sensitivity of K.T.F.R. is affected by the time and temperature of baking, and that the sensitivity drops drastically for films below 0.8μm in thickness.

In figure 2.13, the two negative resist techniques used in the project are described.

The first technique, used in the majority of applications, has a resist thickness of 2.5 μm, which is obtained by



Application and removal of Kodak Thin Film Resist

Figure 2·13

applying the resist at full strength. In applications requiring an improved resolution, (for narrow gaps etc.), better results are obtained by using a 1 μm thick film, obtained by diluting the resist with thinner (3 parts resist to 1 part thinner). This decrease in resist thickness increases the pinhole density, however, and should only be used where the improved resolution is essential.

The main features of the process are;

1. due to the resist being hydrophobic, the substrate should be baked at 70°C for 5 minutes immediately prior to the resist application, to drive off the surface water vapour[58].
2. to minimise undercutting during subsequent etching stages, the resist is post-baked at 70°C for 15 minutes (sect. 2.4.8).
3. the resist can be removed by use of a negative resist stripper (e.g. Chemical Processes 13LS stripper)[60]. The substrate is immersed in the stripper for 60 seconds. The stripper is then removed by washing the substrate thoroughly in a stream of cold water, with subsequent rinsing in I.P.A.. The substrate is finally spun dry. The stripper is an acidic solution and care must be taken with very thin films to prevent over-attack of the surface. The stripper can be used in the majority of applications, apart from situations where removal of an oxide film may cause damage to some other part of the circuit. Caution must, therefore be exercised in the presence of copper films (e.g. chapter 7). Under these conditions, the resist may be removed by soaking in trichloroethylene, which may be heated as necessary, or the substrate surface may be gently swabbed with cotton wool to ensure complete removal of the resist.

2.4.8 The effect of resist post-baking times on undercutting of copper films.

Several samples of 2.5 μm thick copper films were

prepared, and AZ 111 resist applied by the static-flood technique, and spun at 10,000 r.p.m. for 20 seconds. The resulting photoresist layer was baked for 15 minutes. A test mask of 125 μm lines and spaces was then aligned and the resist exposed to ultraviolet light for 15 seconds. The resist was developed for 60 seconds in AZ 303 developer, diluted 1 : 4 with water. The resulting films were post-baked at 70°C for times ranging from between zero and 15 minutes, and the films then etched in sulphate etchant (Appendix 2.4), using dip etching techniques.

The nominal line width of the mask was measured, and the actual line width was also measured, as shown in figure 2.14. The difference between the two measurements was taken as the undercutting during the etching stage. All line width measurements were made on a Reichart Metaplan Metallurgical microscope (with television camera and 20" monitor screen), and had an accuracy of ± 1 μm. The results, summarised in figure 2.15, indicate that the degree of undercutting decreases with increase in post-baking time. Increased post-baking leads, however, to greater difficulty in removing the resist layers, especially with negative resists. Therefore, in these circumstances, the bake time and temperature must be carefully controlled if stripping difficulties are to be avoided. However, no difficulty has been encountered removing the resists by the methods indicated in sections 2.4.6 and 2.4.7, providing the resist application details have been rigidly adhered to.

2.4.9 Etching.

To define conductor and dielectric areas using conventional photolithographical techniques requires etching of the deposited materials. However, techniques were developed during the course of this project (Chapter 7), which have eliminated the need for etching the dielectric materials, and therefore the only etchants which will be discussed at this stage, are the metal etchants, which are tabulated in Appendix 2.4.

All etchants are filtered to 0.5 μm prior to use.

(a) Nominal line width w taken from the photographic mask

(b) Degree of undercutting Δ taken from the etched copper line

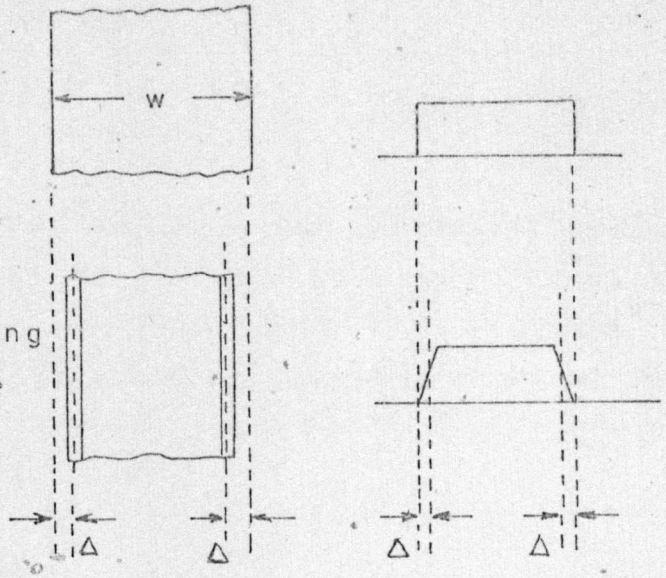


Figure 2·14 Definition of the degree of undercutting

Undercutting of copper films

film thickness 2·5 μm ; Photoresist AZ 111 (0·6μm)

Sulphate etchant applied by dip techniques (Appendix 2·4)

sample	Post-bake time (minutes)	Nominal line width w (μm)	Degree of undercutting Δ (μm)	Mean undercutting (μm)
1	—	125	15·5	
2	—	"	13·9	
3	—	"	15·7	14·87
4	—	"	14·5	
5	—	"	14·75	
6	5	"	6·1	
7	5	"	6·3	
8	5	"	5·8	6·12
9	5	"	5·5	
10	5	"	5·9	
11	15	"	2·5	
12	15	"	2·9	
13	15	"	2·1	2·44
14	15	"	2·6	
15	15	"	2·1	

Figure 2·15 The effect of post-bake times on the degree of undercutting of etched films

Gold etchant.

The gold etchant is adequate for most applications, but it must not be used in the presence of copper films, which it attacks (Chapter 7). Due to the opaque nature of the etchant, best results are obtained by applying a jet of etchant from a wash bottle, with frequent rinses with filtered water, also dispensed from a wash bottle.

Chromium etchant.

The chromium etchant, in general, presents few problems, although the sodium hydroxide content must be strictly controlled if thick chromium layers are used with AZ 111 photoresist. (The developer of which is a buffered pctassium-hydroxide solution). The etchant also reacts with copper etchant (ferric chloride) to form an insoluble deposit, and therefore it is essential that all remains of copper, and the copper etchant, are removed by washing the substrate thoroughly in water, before etching the chromium (or vice versa).

Copper etchant.

The most common etchant for copper is ferric chloride. As previously stated, however, the etchant causes problems in contact with the chromium etchant. It has also been shown (sect. 2.4.10) that ferric chloride produces severe under-cutting, which can be reduced if the sulphate etchant (Appendix 2.4) is used in preference. Therefore. it is advisable at all times to use the sulphate etchant and also to dispense the etchant from a wash bottle, rather than using a dip-etching technique, as this also effectively reduces the amount of undercutting (sect. 2.4.10).

2.4.10 The effect of the copper etchant on undercutting of copper films.

Several samples of 2.5 μm thick copper films were prepared on microscope slide substrates, and AZ 111 resist

applied as described in section 2.4.6. A test mask of 125 μm lines and gaps was exposed, and the photoresist developed accordingly. The samples were then etched using the two copper etchants (Appendix 2.4), in each case using both dip-etching techniques and by dispensing the etchant from a wash bottle. The degree of undercutting was then measured, as indicated in section 2.4.8, and the results are summarised in figure 2.16.

From this figure, it can readily be seen that there is a significant decrease in undercutting if the etchant is dispensed from a wash bottle, rather than using dip-etching techniques. This is due to the etchant flowing, for the most part, at right angles to the photoresist. The increased agitation of this technique also decreases the etching time slightly. The sulphate etchant was found to produce less undercutting than the ferric chloride, although there appears to be no reason for such an occurrence.

2.4.11 Plating.

Before commencement of plating, the surfaces to be plated must be scrupulously clean, and where possible, this should be achieved by the cleaning cycle of figure 2.11.

In heavily oxidised copper films, the detergent soak can be replaced by soaking in Neutra Clean 68[61] at 20°C, which is a soak cleaner for copper films, containing both acids and detergents, and which removes oxide layers. It should not, however, be used where removal of an oxide film may cause subsequent damage to the rest of the circuit (Chapter 7).

In situations where the plating is done through a photoresist mask, the solvent stages, of course, must be eliminated, and where the circuit is of a delicate nature, the ultrasonerating stages should be reduced or eliminated. The objectives, therefore, should be to include as many stages of the cleaning process as possible, without damaging the masking or any part of the circuit.

Plating solutions.

A primary rule worth noting at the outset, is that

Undercutting of copper films

film thickness 2·5 μm ;

photoresist AZ 111 (~0·6 μm) ;
post-bake time 15 minutes :

Sample	Etchant	Application of etchant	Nominal line width	Undercutting μm	Mean undercutting
1	Ferric Chloride	Dip	125 μm	11·5	11·78 μm
2				13·2	
3				10·6	
4				12·5	
5				11·125	
6	Ferric Chloride	Jet	125 μm	6·1	6·12 μm
7				6·3	
8				5·8	
9				5·5	
10				6·9	
11	Sulphate	Dip	125 μm	2·5	2·44 μm
12				2·9	
13				2·1	
14				2·6	
15				2·1	
16	Sulphate	Jet	125 μm	1·0	0·65 μm
17				—	
18				1·5	
19				0·75	
20				—	

Figure 2·16 The effect of etching technique on the degree of undercutting

the introduction of hard water into any plating bath should be avoided, since calcium and magnesium salts give precipitates which have a deleterious effect on the plated finish. Therefore, all baths should be made-up, and maintained, using deionised water. Additionally, the solution should be filtered immediately prior to use.

In an attempt to reduce microwave conductor losses, several different plating solutions were investigated, namely silver, copper and gold (in order of highest bulk conductivity). Initially, therefore, bright silver plating solutions were investigated, and in particular, Elfit plating solution[62]. To obtain consistently bright deposits using this solution, the bath conditions had to be strictly controlled[63] and the solution also proved unsuitable for small batch productions, due to rapid bath deterioration whilst not in use.

Similar problems were also encountered with other commercial silver plating solutions.

Excellent results were obtained using a copper-sulphate bath, which required the minimum of maintenance and produced reproducible results. The deposits were, however, dull in nature, and had a fairly rough surface (C.L.A 0.045μm). The surface roughness could be decreased by decreasing the current density, but larger improvements were made at a later date, by adding leveller, conditioner and brightener[64] to the solution. Although this complicated the bath maintenance, consistent results could still be obtained with the minimum of operational difficulties.

To obtain bright copper plate, the optimum conditions were found to be those given in Appendix 2.5, of which the most critical is the voltage. To obtain the necessary voltage difference, an electrode separation of 12" was required. For microstrip circuits, two sides of the substrate must be plated, and to ensure a uniform deposition, it is advisable to plate both sides of the substrate at one time. The most suitable electrode configuration was found to be that shown in figure 2.17. It has also been shown[65] that improved results can be achieved by applying a steady stream of electrolyte at right angles to the direction of current flow, and this feature was also incorporated. The conductivity of the bright copper

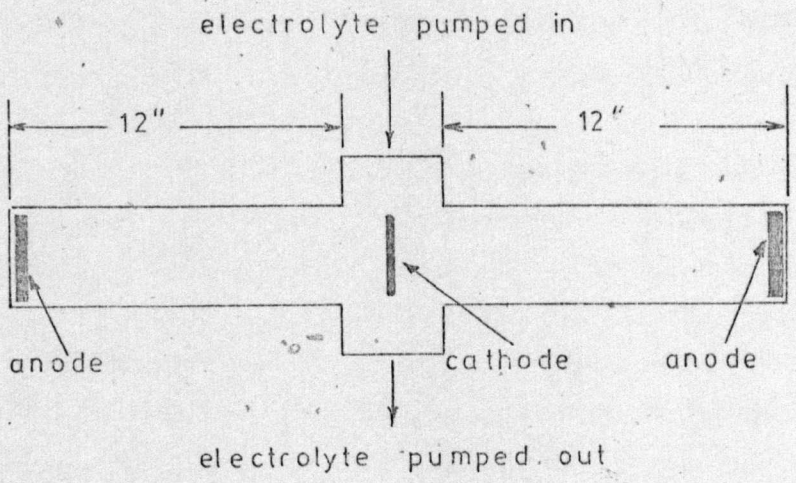


Figure 2-17 Copper plating bath

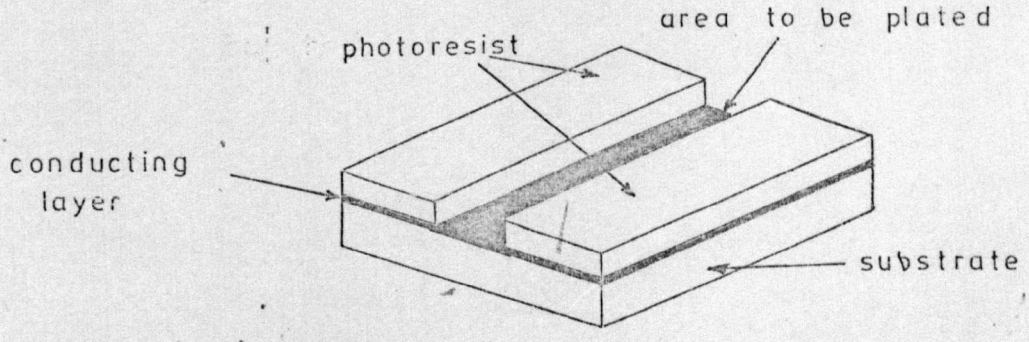


Figure 2-18 Plating-through-resist technique

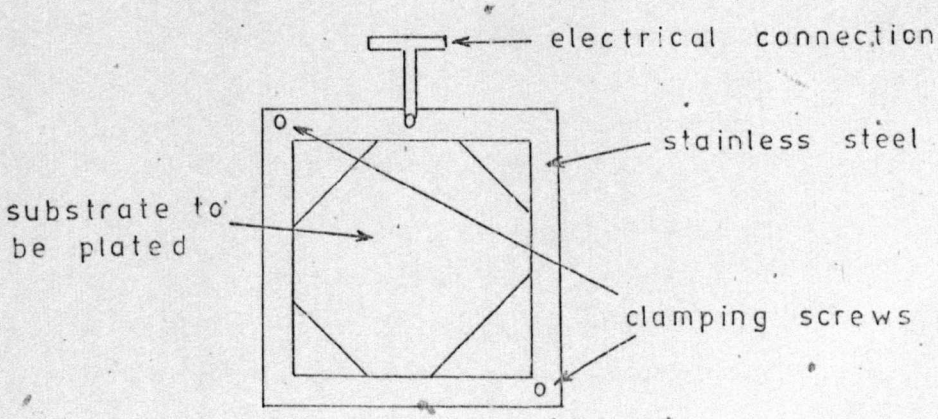


Figure 2-19 Plating jig for obtaining uniform electroplate deposit

plate is 46.7×10^6 Cond^7 units, and the C.L.A. is 0.03 μm.

A comprehensive study of the microwave conductivities of deposits obtained from various plating solutions using varying bath conditions, is given by Butlin[7,28], and it is from these results that the values of conductivities of the plated deposits are obtained.

In certain situations, it is advisable to use gold as the main plating material, but for the applications described in this thesis, the gold plate is used only in the form of a gold "flash" on copper electroplated films, to give protection against oxidation and to produce a more robust mating surface for the electrical connectors. The thickness of the gold flash is generally 0.1 μm, but could be up to 0.25 μm where additional protection is necessary because of electrical contacts which have to be continually made and removed.

Bright gold deposits, with a conductivity of 34.5×10^6 Cond^7 units can be very easily obtained from P.M.D. Gold Transtherm solution[60]. This produces a higher quality deposit than that obtained from Electroless EL 221 gold[67], which was also investigated. 66?

Connection to the cathode.

Uniformity of the electroplate is directly related to the uniformity of current flow at the cathode, and therefore, where connections to the cathode are made, the current flow must be arranged to be as uniform as possible. This was most easily attained by electroplating through a layer of photoresist. In this situation (figure 2.18), a continuous conducting layer exists below the photoresist, and current can therefore be fed into the areas to be plated, in all directions, resulting in a more uniform current distribution. This is, of course, dependent upon making electrical connection to the substrate in such a way that a uniform current distribution can exist. A satisfactory method of ensuring this was to connect the substrate in a clamp as shown in figure 2.19.

The grain size of the deposit is a function of the current density, and for sharply defined edges (e.g. narrow gaps), low current densities are used. This is because the

microcircuit distribution becomes less uniform at increasing current densities[68]. This is also important in plating-up through photo-resist, as higher current densities tend to seek-out pinholes in the resist film.

For the plating of small samples, dummy electrodes, which are considerably larger than the area to be plated, are used to ensure that the current density can be accurately defined.

Due to the importance of a good surface finish of the electrodeposited material, both chemical and electrolytic polishing techniques were investigated, but they were discarded because of the amount of deposit removed in the process - up to 1500 μm in 90 seconds, which is clearly impractical for thin films.

2.5 Conclusions.

In this chapter, the basic processing techniques to be used throughout the project have been discussed in considerable detail.

The main conclusions are;

1. thin film techniques are to be employed.
2. the performance of the photoreduction camera is better than that required for M.I.C. techniques in general.
3. improved film adhesion is obtained if substrates are glow-cleaned prior to the deposition.
4. the post-baking time for the resist film is critical if undercutting during subsequent etching stages is to be minimised.
5. when etching copper, improved resolution and reduced undercutting can be achieved by using the sulphate etchant dispensed from a wash bottle, in preference to either the ferric chloride etchant, or dip etching techniques.
6. the conductors should be electroplated to a thickness of at least 2 skin depths, using bright copper plate, deposited from an acid copper bath, and then should

be protected by a 0.1 μm thick layer of gold, deposited from a P.M.D. Transtherm solution.

7. an indication of the overall system performance can be obtained from figure 2.20 and 2.21. Figure 2.20 shows a 6.0 μm gap etched in an 0.25 μm thick film of evaporated copper on a quartz substrate, and figure 2.21 shows an S.E.M. photograph of an 11 μm wide gap in a 5 μm thick film of electroplated copper on a quartz substrate.

This latter figure depicts the most stringent requirements anticipated for this project.

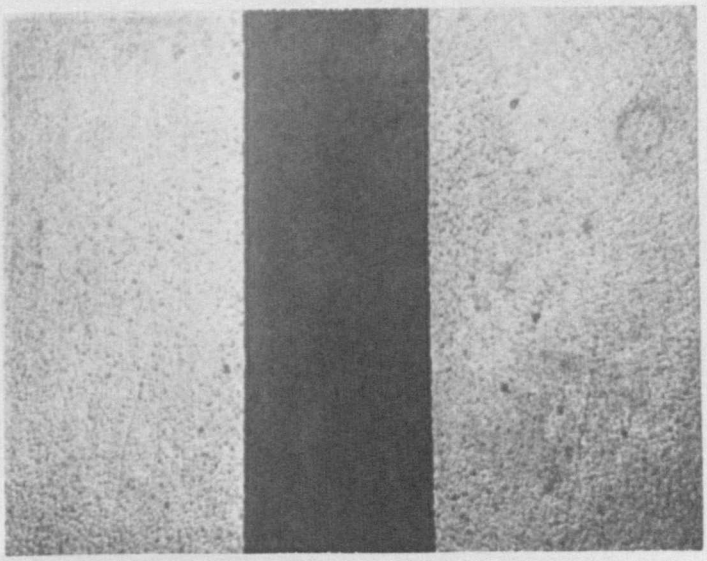
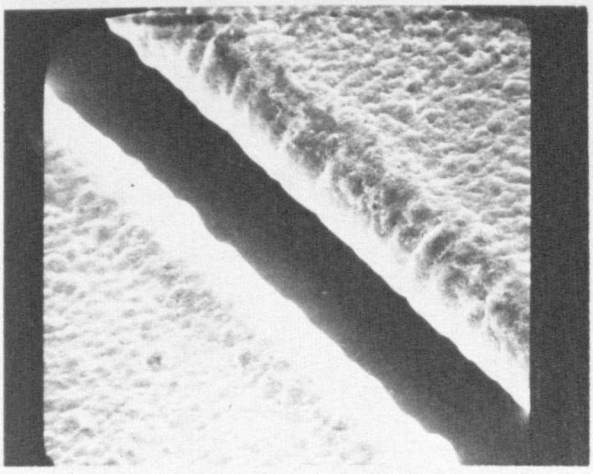


Figure 2·20 6 µm gap etched in an 0·25 µm thick film of evaporated copper

Figure 2·21 11 µm gap defined in a 5 µm thick film of electroplated copper



3. TRANSMISSION CHARACTERISTICS OF MICROSTRIP LINES.

3.1 Introduction.

The technique devised for the measurement of thin film overlay capacitors at X band, relies on microstrip as an interconnecting medium between the L.E. and the measurement equipment. To permit accurate measurements of the L.E. properties, therefore, the microstrip characteristics (viz. phase velocity β, and characteristic impedance Z_o), must be known to a high degree of accuracy.

This chapter discusses methods currently available for evaluating these microstrip properties. It presents a detailed account of the techniques adopted in this project to determine the characteristics, and submits results obtained by the author, for the properties of microstrip lines on quartz substrates up to 12 GHz. These results are used substantially at later stages of the project, for the design of microwave circuits, and in particular, in the design of a technique for measuring L.E. overlay capacitors.

3.2 Historical review.

3.2.1 T.E.M. solutions of the transmission characteristics.

A microstrip line (figure 1.1), is a two conductor transmission line consisting of a narrow conducting strip deposited on to a thin substrate, which has its other side entirely ccated with a conducting ground plane.

Due to the 2-dielectric nature of microstrip, the rigorous determination of the transmission parameters is extremely complicated, and most theories to date rely on simplifying approximations.

The electrical and magnetic fields associated with microstrip (figure 3.1), show a discontinuity at the air-dielectric interface under normal dynamic conditions. The propagation mode is not, therefore, a simple T.E.M. mode, and there are, in fact, components of both the electric and magnetic fields in the direction of propagation.

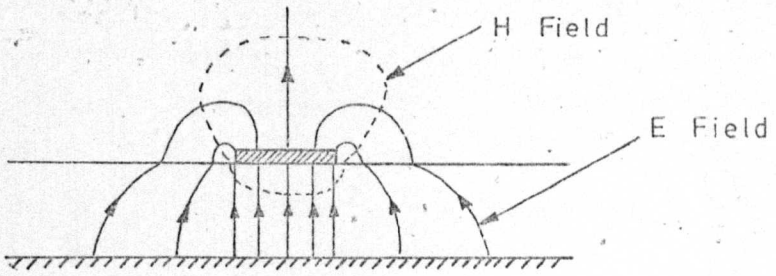
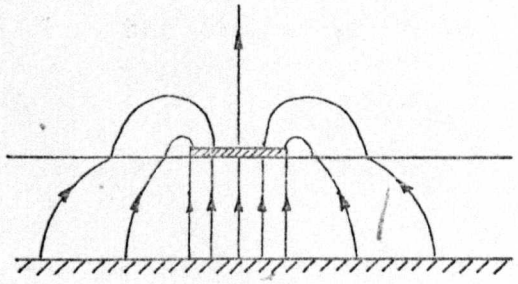
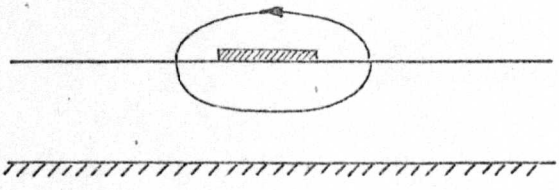


Figure 3·1 Microstrip field diagram — dynamic configuration



(a) E field



(b) H field

Figure 3·2 Microstrip field diagram — static configuration

However, when the dielectric thickness is much shorter than a wavelength, the system approximates to the static configuration of figure 3.2, or a simple T.E.M. mode.

For this reason, and due to the complexity of determining the rigorous, non- T.E.M. solutions for the transmission parameters, the majority of theories at the outset assumed quasi-static T.E.M. approximations.

The first extensive study of microstrip lines for propagation of microwave energy, was published in 1952 by Assadourian and Rimai[69]. Their approximate analysis, involving conformal mapping, provided useful design equations for ratios of strip width to substrate thickness $(\frac{w}{h})$, much greater than unity.

In 1954, Deschamps[70] discussed the possible modes of propagation of a microstrip line. He emphasised that no pure T.E. or T.M. mode solutions were possible, and that the existence of at least one surface-wave mode, resulting from the perturbation of the fundamental T.E.M. mode by the dielectric, could be assumed.

During the same year, Schetzen[71] obtained a T.E.-T.M. mode solution by assuming a longitudinal component of current having a constant amplitude across the width of the strip. This, however, led him to the false conclusion that the phase velocity was constant with frequency.

In 1955, Black and Higgins[72] derived, in a lengthy analysis, an expression for the capacitance per unit length of line.

To overcome the immediate practical design problem, Dukes[73] produced empirical results which were sufficiently accurate for many practical applications, but which neglected the dielectric discontinuity. These results were also inaccurate for the most useful practical cases of microstrip $\frac{w}{h}$ ratios approximately equal to unity.

The main difficulty in obtaining a complete solution, arose from the necessity of taking into account the dielectric discontinuity at the insulator boundary, the fringing fields, the finite conductor size and the radiation losses. The approximate theories, which were based on T.E.M. propagation, accounted for the fringing fields, but neglected the dielectric

discontinuity and the radiation.

Wu[74,75] tried to account for some of these effects, by formulating a pair of coupled-integral equations for the two unknown components of current density that exist in the strip, namely the longitudinal component and the transverse component. However, because of the extreme complexity of his equations, they have never been solved.

In 1958, Brodwin[76] used Van Trier's[77] analysis of a ferrite-filled microstrip line, having a strip width of at least half a wavelength. A simple relationship was obtained between the propagation constant and the applied longitudinal magnetic field for a quasi-T.E.M. mode.

In 1964, Wheeler[78,79] published a conformal mapping analysis of a dielectric-filled microstrip line, which did account for the dielectric discontinuity, but did not rigorously satisfy the discontinuity boundary conditions, and was therefore still a T.E.M. approximation.

Caulton[80] used Wheeler's conformal mapping theory to derive a set of design curves for microstrip lines applicable over a wide range of geometries and substrate materials. Design data was presented for characteristic impedance, wavelength, attenuation, and line width correction for finite thickness conductors.

Schneider[81] developed simple empirical formulae to fit Wheeler's design curves. Schneider's microstrip model assumed T.E.M. propagation, and initially he restricted the dielectric constant of the substrate to unity. He developed a rigorous solution for the characteristic impedance, Z_o, in the form of theta functions, to fit Wheeler's data, and then approximated these expressions by the two simple equations of 3.1 and 3.2.

$$Z_o = 60 \ln_e\left(8\frac{h}{w} + 4\frac{w}{h}\right) \qquad \frac{w}{h} \leq 1 \qquad 3.1$$

$$Z_o = \frac{120\pi}{\frac{w}{h} + 2.42 - 0.44\frac{h}{w} + \left(1-\frac{h}{w}\right)^6} \qquad \frac{w}{h} \geq 1 \qquad 3.2$$

where (figure 1.1) w is the microstrip line width
h is the sustrate thickness.

The maximum error of these approximations from the rigorous theta function solution, is $\pm$ 0.7%, and for the range $0 \leq \frac{w}{h} \leq 10$, the error is less than $\pm$ 0.25%.

The characteristics of microstrip with substrates of dielectric constant other than unity, were then found by defining an effective constant, E_{eff}, such that

$$Z = \frac{Z_o}{\sqrt{E_{eff}}} \qquad 3.3$$

$$\text{and} \qquad \beta = \beta_o \sqrt{E_{eff}} \qquad 3.4$$

where Z_o and β_o are the characteristic impedance and phase constant of microstrip lines with substrate dielectric constant, e_r, of unity, and Z and β are the corresponding functions for $e_r = 1$.

Schneider then derived an empirical expression (equation 3.5) for E_{eff} from Wheeler's data, which had an accuracy of $\pm$ 2% for all $\frac{w}{h}$ ratios.

$$E_{eff} = \frac{e_r+1}{2} + \frac{e_r-1}{2} (1 + 10\frac{h}{w})^{-\frac{1}{2}} \qquad 3.5$$

where e_r is the substrate dielectric constant.

As a result of Schneider's equations, a value of characteristic impedance Z could be calculated to within $\pm$ 1.25% for $0 \leq \frac{w}{h} \leq 10$, and a value of phase velocity β, to within $\pm$ 1%, from the rigorous solution of the T.E.M. approximation using theta functions.

Measurements by Caulton[80] showed good agreement with results derived from Wheeler's work up to 4 GHz, confirming that the T.E.M. model (and the static solution) were sufficiently accurate for the lower microwave frequncy range.

Further theoretical analyses[82-91], mostly numerical in nature, have yielded more accurate T.E.M. approximations for the characteristics of microstrip, but in general, they

are not sufficiently adaptable for simple design purposes, without the aid of a computer.

Schneider's equations (3.1-3.5) are sufficiently accurate for normal circuit applications, and due to the lack of a more accurate alternative, these equations were used as a basis for all microstrip circuit design in this thesis.

At a later date in the project, two Fortran programs became available[92] for evaluating the transmission properties of microstrip using the quasi-static approximation of Bryant and Weiss[88] and of Wheeler[78,79], but they were not available sufficiently early to be incorporated in this work.

3.2.2 Variation of E_{eff} with frequency.

Further experimental work at higher frequencies, yielded larger discrepancies from Wheeler's theoretical analysis, than did Caulton's work at 4 GHz. Seckelmann[93] noted that the effective dielectric constant increased with increase in frequency i.e. that microstrip was dispersive. This was also reported by others[94-98], and is attributed to the non-T.E.M. nature of propagation of microstrip, and in particular, to the longitudinal field components which increase in magnitude as the frequency increases[99]. The deviation from Wheeler's T.E.M. analysis, due to the frequency variation of E_{eff}, approximates 7% at 10 GHz for alumina substrates, and therefore, the accurate determination of the characteristics of microstrip at X band, using Wheeler's T.E.M. analysis alone, are clearly impossible.

3.3 Current methods available for determining the characteristics of microstrip.

Due to the lack of a suitable alternative theory more accurate than Wheeler's, and also to the lack of a theoretical analysis to predict the variation of E_{eff} with frequency, alternative techniques to accurately determine the transmission characteristics of microstrip at X band were required.

The approach which was generally being adopted at the outset of the project, was to assume that equations 3.1 -

3.4 were basically correct (as has been shown to be the case for the lower microwave frequency range), and then to obtain, by experimental methods, the variation of E_{eff} with frequency. In this way, both the characteristic impedance, Z, and the phase constant, β, could be determined, with their accuracy being limited predominantly by the accuracy with which the effective dielectric constant, E_{eff}, could be measured.

As alternative approaches for determining microstrip characteristics, interest was also being shown in the direct measurement of characteristic impedance, and in theoretical predictions of the variation of E_{eff} with frequency.

The objectives of this chapter, therefore, are to investigate the methods which were available at the commencement of the project for determining the characteristics of microstrip, and thereafter, to accurately evaluate the characteristics of microstrip lines on quartz substrates, using suitable techniques. The results of these measurements will then be used as a basis for the accurate design of microstrip circuits used in the remainder of this project.

The basic approaches outlined previously which will be investigated in this chapter, and which will be discussed in detail in the next section, are therefore;

1. the determination of E_{eff} by practical measurement techniques.
2. the direct measurement of characteristic impedance.
3. the theoretical determination of E_{eff}.

3.3.1 Determination of E_{eff} by practical measurement.

Several measurement techniques have been developed in the past for the measurement of E_{eff}, but the majority of published data to date, relates only to microstrip lines on alumina substrates. These measurement techniques can generally be classified into two main categories - resonant and non-resonant methods.

1. Resonant methods

   a) ring resonators
   b) open-circuit resonators
   c) short-circuit resonators

2. Non-resonant methods

   d) transmission measurement
   e) nodal shift measurement

The advantages and disadvantages of each of these methods will be discussed in detail, to enable measurement techniques to be adopted for the particular application required for this project.

Resonant Methods.

1. Ring resonators.

Ring resonators were first described by Troughton[95,100] and then subsequently by others[101,102]. Their main advantage is that, unlike linear resonators, no end-effects need be considered. Arnold[103] has shown that, of the techniques investigated by him, the ring resonator was the most accurate resonant-line technique (but he did not consider Mehmet's method, section 3.4.2), and that the errors increased at extremes of microstrip geometries. Wolff[101] has shown that for low impedance lines, and for low e_r substrates, the effect of the curvature of the ring produces significant errors, and even for the improved theoretical model he describes, accuracies are still limited. In general, ring resonators are not recommended for low e_r, low Z_o lines, as, for reasonable accuracy, prohibitively large substrates are required. For this particular application, as the dielectric constant of quartz is low, and predominantly low impedance lines will be investigated, this technique was not considered further.

2. Open-circuited resonant lines.

In open-circuited resonant line techniques in general, the wavelength measurement is complicated by the reactive end-effects, and the unloaded Q by the radiation losses from the open circuits. Both of these factors are functions of frequency, conductor width, substrate thickness, and the length of the resonator in wavelengths. If accurate measurements are to be made, it is difficult, and time consuming, to adjust measured data for these perturbations.

One method, described by Deutsch[104], and used by others[105], effectively eliminates these end-effect inaccuracies. This is achieved by using two open-circuited resonators of exactly similar geometries on the same substrate, but with one resonator approximately twice the length of the other. The resonant frequencies are then very close to each other at the frequency of interest. Under these circumstances, the end effects are equal, providing the difference in resonant frequencies of the two lines is small.

Such a method is then limited in accuracy only by the accuracy with which the resonant frequency can be measured, and is typically $\pm$ 0.2%.

3. Short-circuited resonant lines.

Short-circuited resonators have been described by Mehmet[19,106], and, providing the fringing fields at the ends of the resonator are effectively short-circuited, measurement accuracy is limited only by the accuracy with which the resonant frequency can be measured. This technique has the advantage over other techniques, of having an extremely simple resonator, which results in simple construction and simple theoretical analysis.

Non-resonant techniques.

4. Transmission measurements.

Transmission measurements have been described by

Napoli[96] and Caulton[98], in which the phase of a non-dispersive line (coax.) is compared to that of microstrip. The measurements are limited in their accuracy, however, by the uncertainties associated with the transition from the coaxial structure of the test equipment to the microstrip configuration.

5. Nodal shift technique.

The nodal shift technique was initially described by Seckelman[107]. The method investigates the phase of the reflection coefficient of open-circuited or short-circuited transmission lines. The theory is relatively complex, and the measurement tedious, but the technique has the advantage of being able to determine both the effective dielectric constant and the line impedance independently.

3.3.2 Direct measurement of characteristic impedance Z.

Two techniques were considered applicable at the commencement of the project for the direct measurement of the characteristic impedance of microstrip lines. These were

1. time-domain reflectometry
2. nodal shift technique

1. Time-domain reflectometry.

The simplest and most direct method for measuring the impedance of microstrip is by time domain reflectometry (T.D.R.). The frequency, f, at which the results are valid, is determined by the rise time, t_r, of the system[108-9]

$$f = \frac{0.35}{t_r} \qquad 3.6$$

The T.D.R. available was the Hewlett Packard 1415A, with a system rise time of 150 picoseconds. Therefore results are valid up to 2.33 GHz, or fundamentally the low frequency T.E.M. solution. The technique, using the equipment available, is suitable therefore, only as a quick

check of the T.E.M. impedance and yields no information as to the dispersive nature of microstrip.

2 Nodal shift technique.

Section 3.3.1 - 5.

3.3.3 Theoretical determination of E_{eff}.

At a later date in the project, many theoretical analyses of microstrip dispersion became available. The only theories however, which were of practical design use (to those not possessing the computer programs for the vast number of numerical solutions available[110-119]), were those of Schneider[120] and Jain[121].

These theories were claimed to be accurate to only 3% and 5% respectively, which were, therefore, considerably less accurate than some of the methods available for the direct measurement of E_{eff}, and of insufficient accuracy for the requirements of this project. However, it was considered of interest to compare the results derived from these theories with the results obtained from the practical measurement techniques.

3.4 Detailed analysis of the techniques adopted for the determination of microstrip properties.

3.4.1 Introduction.

The technique which appeared most suitable for the measurement of the properties of microstrip lines on quartz substrates, was Mehmet's method (sect. 3.3.1-3), due to the accuracy, the simple resonator construction, and the simple theoretical analysis. However, being a new, virtually untested technique, it was considered advisable to compare at least some of the results using this method, with results obtained using another technique. The only other measurement method which could be adopted with the minimum of alterations to the resonators required for Mehmet's method, was the nodal shift technique.

Mehmet's method requires a resonant line short-circuited at both ends. By removal of one of these short circuits, the same lines could be used for the nodal shift technique for the determination of both E_{eff} and Z.

Further, if the remaining short circuit were to be removed, and a matched load connected in its place, the characteristic impedance of the microstrip lines could be measured using T.D.R. techniques. Therefore, from one linear transmission line structure, three independent measurement techniques could be employed to determine the microstrip characteristics, with the minimum of modifications to the circuit.

The basic measurement procedure was therefore;

1. to construct a linear resonator with both ends short-circuited, and to measure E_{eff} using Mehmet's method.
2. to remove one of the short circuits, and to measure the impedance and E_{eff} by the nodal shift technique.
3. to remove the remaining short circuit, and to measure the impedance using T.D.R. techniques.

In the following section, a detailed account of the theories of these particular techniques, and the practical measurement details will be presented.

3.4.2. Mehmet's method.

A full description of the theoretical aspects of this technique is given in Appendix 12.1, with selected practical measurement details. It is not considered necessary, therefore, to repeat the description, and only additional measurement details will therefore be presented at this stage.

Experimental procedure.

Short-circuited resonant lines of impedances varying from 15 - 65 ohms (calculated using equations 3.1-3.5), were prepared on 1"x1"x0.020" quartz substrates as described in Appendix 3.1. The thickness of each substrate was measured

prior to processing, by means of a Tesamaster direct reading micrometer, with an accuracy of $\pm$ 0.75 μm.

The substrates, supplied by Gooch and Housego, have rounded edges, which facilitates the formation of short circuits, by preventing the deposited films from breaking at the sharp edge discontinuity. However, this leads to difficulties in determining the exact position of the substrate edge, and can lead to errors in line length measurement of up to 2% if the microstrip lines are shortcircuited. This in turn introduces an error of up to 1% in E_{eff}. Therefore, to avoid this error, the substrate edges are polished prior to processing to remove the bevel virtually completely.

The microstrip line dimensions were measured on a Zeiss Toolmaker's Precision Microscope, to an accuracy of $\pm$ 2.5μm.

The only electrical parameter to be measured was the resonant frequency, f_{ox}, which was measured using the coaxial reflectometer of figure 3.3. The most accurate method of determining f_{ox}, was to display part of the resonant peak on the X-Y recorder, and to adjust the oscillator so that the sweep was symmetrical about the resonant frequency. The sweep was then triggered, and an X-Y recording taken, noting the sweep start and stop frequencies. By linear interpolation of the resulting calibrated plot, the resonant frequency could then be calculated.

For each susbstrate, five measurements of the resonant frequency were taken, and in between each measurement, the substrate was completely removed from the test jig. The resulting repeatability of measurement of the resonant frequency was $\pm$ 0.01%.

Then, knowing the resonant frequency, f_{ox}, the mode number, n, the physical line length, l, and the velocity of light, c, the effective dielectric constant could be determined using equation 3.7 (Appendix 12.1).

$$E_{eff} = \left(\frac{nc}{2lf_{ox}}\right)^2 \qquad 3.7$$

The results of the measurements on quartz substrates using this technique are discussed in section 3.5.

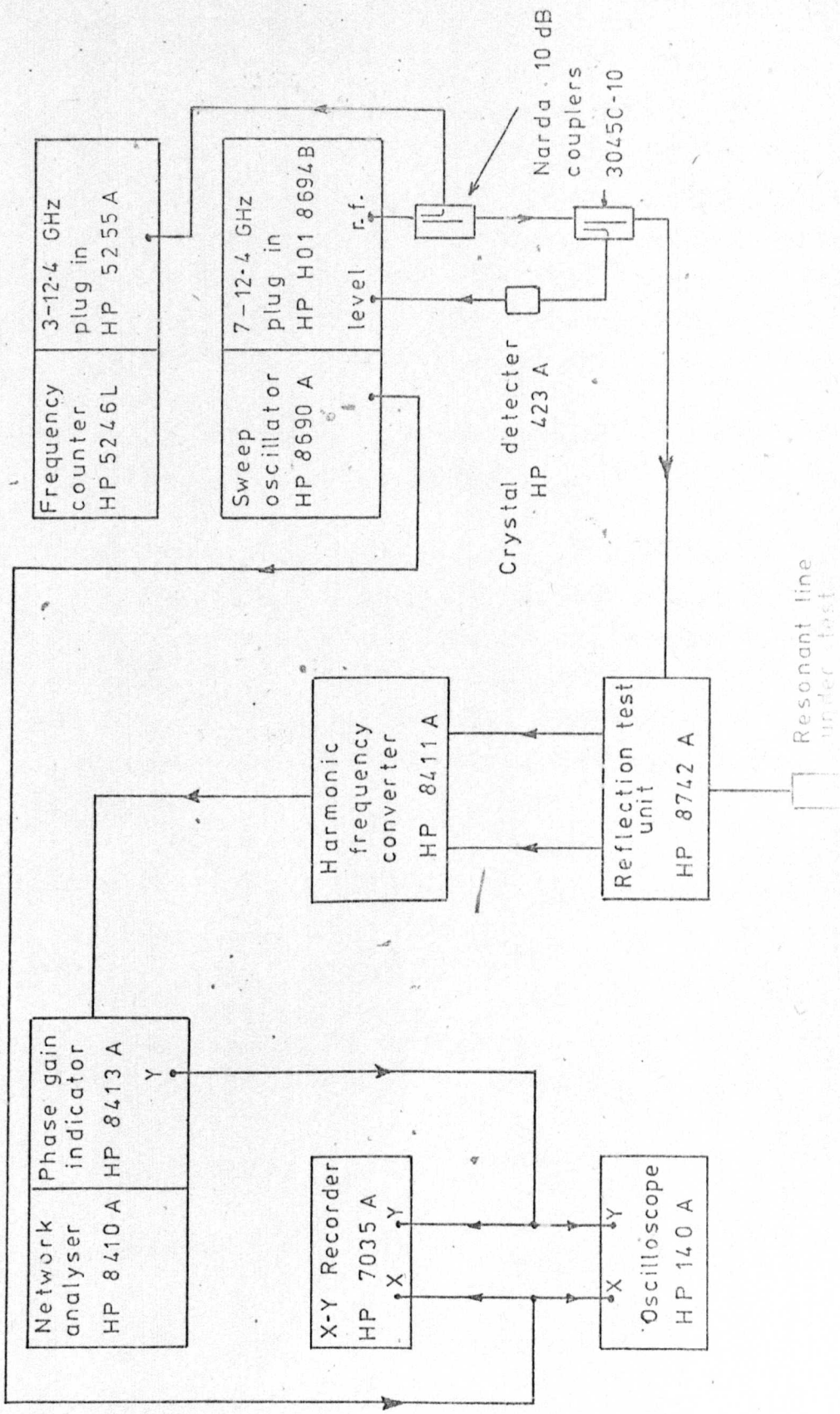


Figure 3·3 X band coaxial reflectometer

3.4.3 Nodal shift technique.

This technique was originally described by Seckelmann[107]. Using a coaxial slotted line (figure 3.4.a) of characteristic impedance, Z_o, and phase constant, β_o, the position, A, of a particular minimum from a reference short circuit position, C, is measured. The reference short circuit is then replaced with the microstrip line (figure 3.4.b), of length l_e, impedance, Z_e, and phase constant, β_e, terminated in a short circuit.

The new position, B, of the reference node is then located, and the shift of the minimum, l_o, towards the load is measured.

In this situation, the impedance at the point, A, looking towards the load is $jZ_o \tan \beta_o l_o$, and the impedance at the reference short circuit position, C, looking towards the load is $jZ_e \tan \beta_e l_e$. With the supposition that the junction between the two lines, Z_o and Z_e, contains no parasitic reactances or impedances, the resulting condition for continuity at the junction, C, is

$$j Z_o \tan (\beta_o l_o + n\pi) = j Z_e \tan (\beta_e l_e) \qquad 3.8$$

where $n = 0, \pm 1, \pm 2$ etc..

The term n indicates an infinite number of solutions, and the solution with n = 0, has the most significance.

Determination of E_{eff}.

If a plot of $\frac{\beta_o l_o}{\beta_e l_e}$ against $\beta_e l_e$ is made (figure 3.5), it can be seen that $\frac{\beta_o l_o}{\beta_e l_e} = 1$ when $\beta_e l_e = m\frac{\pi}{2}$ (m=1, 2 etc.), because of the periodicity of the tan function. Therefore, at these points $\beta_e l_e = m\frac{\pi}{2}$

i.e. $$\frac{\omega l_e \sqrt{E_{eff}}}{c} = m\frac{\pi}{2}$$

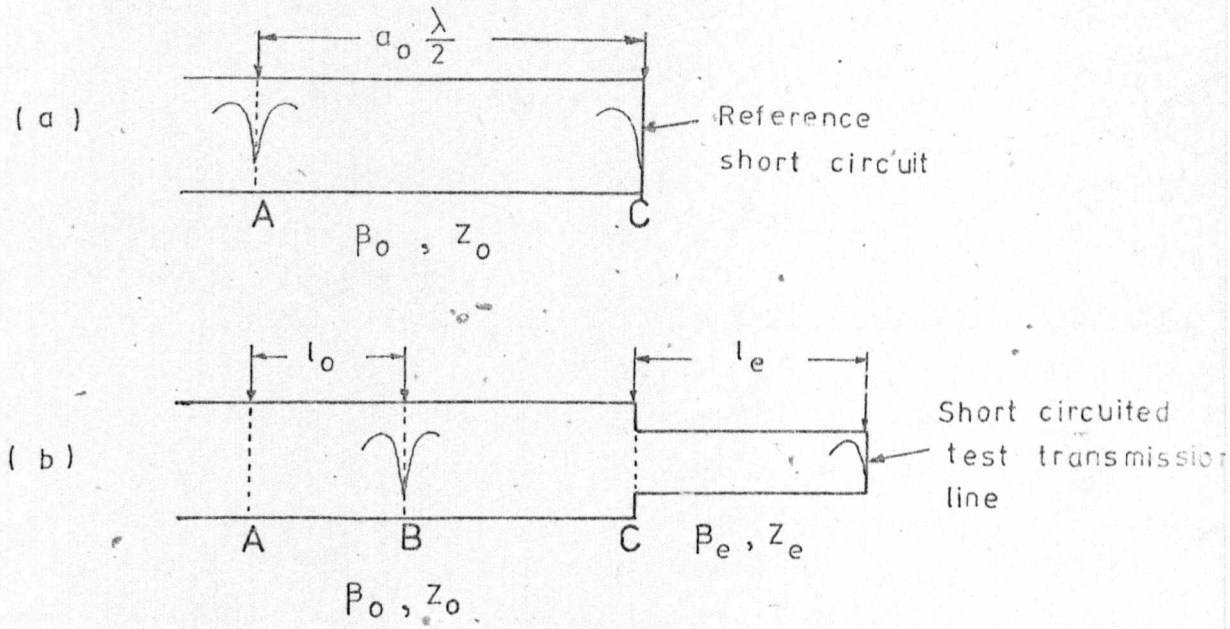


Figure 3·4 Theory of Nodal Shift technique

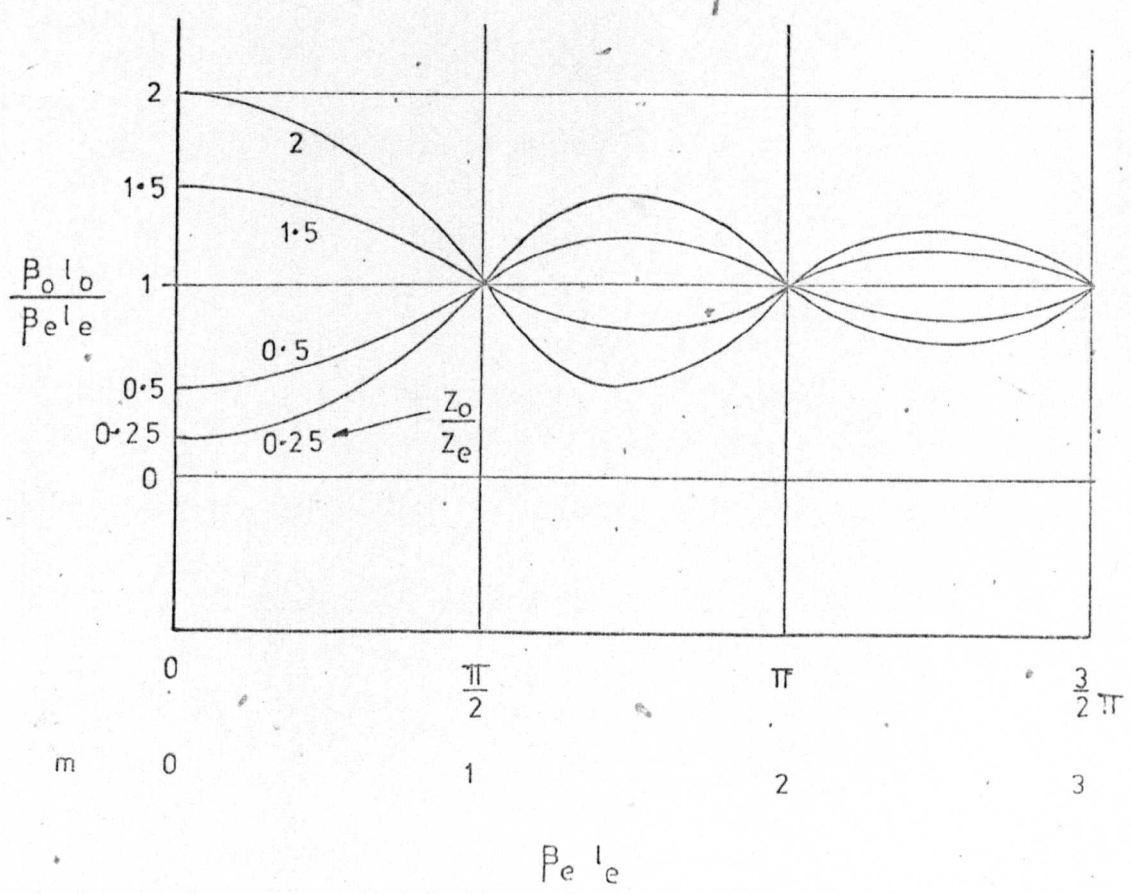


Figure 3·5 Nodal Shift Plot

where c is the velocity of light.

Therefore,

$$E_{eff} = \left(\frac{mc}{4f1_e} \right)^2 \qquad 3.9$$

Therefore, if the line length, 1_e, and the frequency, f, are measured, and m is known, the effective dielectric constant can be calculated.

The paramters $\beta_e 1_e$ and $\frac{\beta_o 1_o}{\beta_e 1_e}$ are inconvenient variables to plot directly, as the measured variables are the nodal shift, 1_o, and the frequency, f. The vertices of the graph of figure 3.5 can, however, be changed in scale without destroying the basic form of the plot, by determining the relationships between the nodal shift 1_o and $\frac{\beta_o 1_o}{\beta_e 1_e}$, and the frequency f and $\beta_e 1_e$.

i.e. $$\frac{\beta_o 1_o}{\beta_e 1_e} = \frac{2\pi f 1_o}{c} \cdot \frac{c}{2\pi f 1_e \sqrt{E_{eff}}} = \frac{1_o}{1_e \sqrt{E_{eff}}}$$

hence $$1_o = \frac{\beta_o 1_o}{\beta_e 1_e} 1_e \sqrt{E_{eff}} \qquad 3.10$$

and rearranging expression 3.9

$$f = \frac{mc}{4 1_e \sqrt{E_{eff}}} \qquad 3.11$$

Therefore, using equations 3.10 and 3.11, the nodal shift, 1_o, can be plotted directly against the measured frequency f. Then by determining the positions at which $\frac{\beta_o 1_o}{\beta_e 1_e} = 1$ from the resulting plot, the effective dielectric constant E_{eff} can be calculated using equation 3.10. The calculated value of E_{eff} can also be related to the frequency at these points, and, therefore, the variation of E_{eff} with frequency throughout X band can be determined.

Determination of the characteristic impedance.

From figure 3.5, it can be seen that the relative amplitudes of the peaks of the nodal shift plot, are uniquely determined by the ratio of $\frac{Z_o}{Z_e}$ i.e. the ratio of the unknown microstrip line impedance to the impedance of the slotted line.

Therefore, by determining the magnitude of the peaks, the unknown impedance, Z_e, can be determined.

Rearranging equation 3.8, and assuming n = 0

$$l_o = \frac{1}{\beta_o} \arctan \left(\frac{Z_o}{Z_e} \tan \beta_e l_e \right) \qquad 3.12$$

The locus of the peaks of the nodal shift plot are then found by evaluating the differential, $\frac{dl}{df}o$, from equation 3.12, and equating to zero. Hence we find (Appendix 3.2)

$$\frac{Z_e}{Z_o} = \frac{\beta_o l_o \sec^2(\beta_o l_o)}{\beta_e l_e \sec^2(\beta_e l_e)} \qquad 3.13$$

The value of $\frac{\beta_o l_o}{\beta_e l_e}$ is given by the ratio of the peak value of the nodal shift to the mean value, at each of the maxima in turn (figure 3.5). Also, $\beta_o l_o$ can be evaluated for each individual peak, knowing the frequency and the nodal shift at that point. Therefore, the unknown line impedance, Z_e, can be calculated using equation 3.13.

Seckelmann[107] presents a series of curves for the calculation of the impedance to simplify the analysis, but it was found to be much more accurate to program the Hewlett Packard Calculator (HP 9100A) to calculate Z_e using equation 3.13, for a given ratio of peak nodal shift to mean nodal shift and frequency.

General experimental details.

The samples used in Mehmet's technique were modified by the removal of one of the short circuits, producing

microstrip lines with one end open-circuited, and the other short-circuited.

Connections to the line were made with the same modified transition as used in Mehmet's method, and the fringing fields at the short-circuited end of the line were again short-circuited by a brass block (Appendix 12.1).

The measurement technique requires a reference short circuit at the input to the microstrip line. As a commercial short circuit at the required reference plane was not available, a suitable short circuit was made from a modified OSM bulkhead mount (type OSM 204CC) as shown in figure 3.6.

The phase variation of the short circuit was measured from 0 - 12 GHz to ensure that there were no spurious phase variations, and a plot of the results is given in figure 3.7. The reference plane of the short circuit was also checked by interpolating between the reference plane of a standard OSM short circuit, and an OSM off-set short circuit, which straddled the required reference plane. Agreement between the two methods was found to be better than 0.8% at 10 GHz.

The measurement system is shown in figure 3.8. The Marconi signal generator was modified to accommodate a fine-frequency control, which permitted the frequency to be set to within $\pm$ 5 kHz of the nominal value.

The position of the minimum on the slotted line was located by determining the point of equal response on either side of the minimum and taking the mean value. For each minimum, the average of 5 measurements was taken at different levels on the response curve to eliminate any non-symmetry of the response.

Maximum accuracy is achieved, for high V.S.W.R. measurements, using large probe penetrations, providing the probe does not shift the position of the minimum[122].

At selected frequencies, the minimum position was measured for various probe penetrations, and no shift was noted within the accuracy of measurement ($\pm$ 0.13mm). On this basis, all subsequent measurements were made with maximum probe penetration.

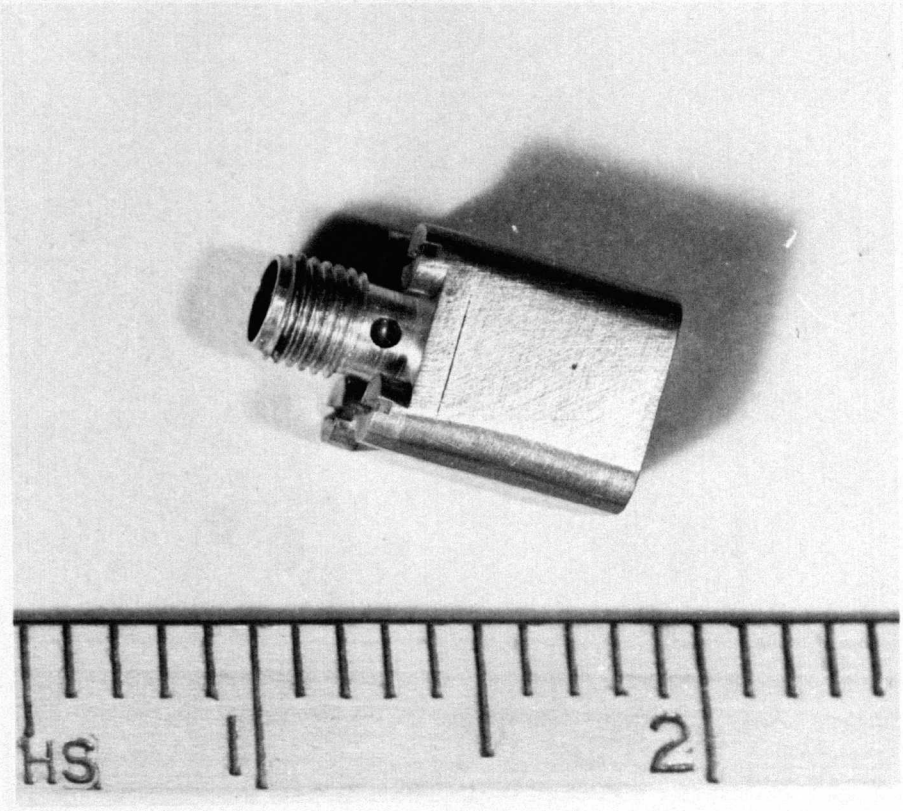


Figure 3·6 Reference short circuit

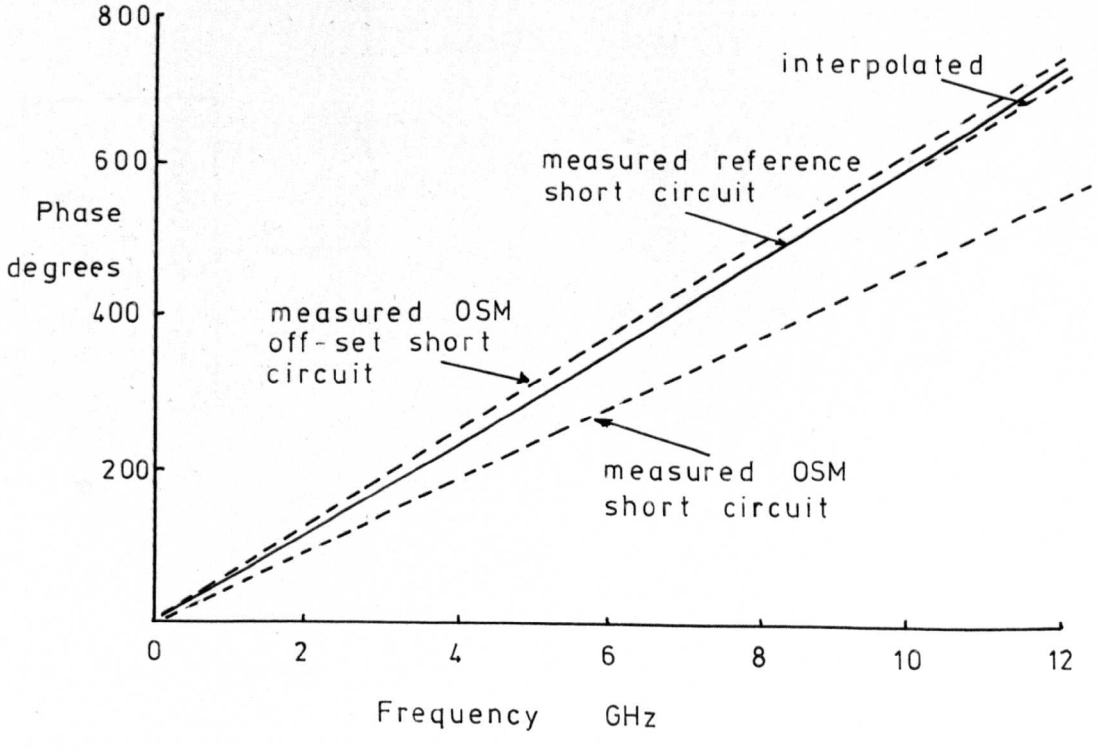


Figure 3·7 Phase variation of reference short circuit

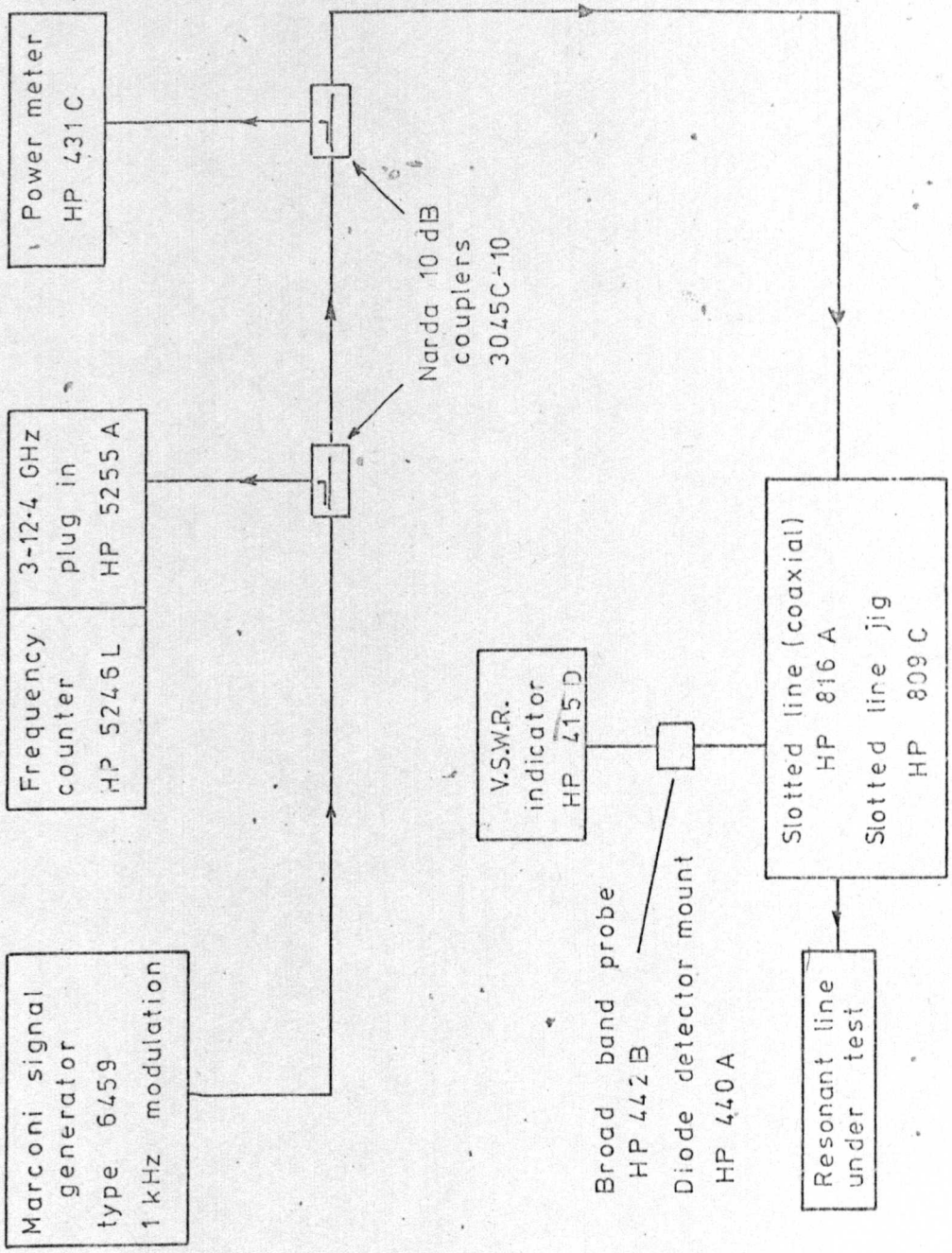


Figure 3·8 Nodal shift measurement system

Experimental procedure.

With the reference short of figure 3.6 as a load, the position of a minimum was located with the aid of the micrometer adjustment. The short circuit was then replaced with the microstrip line under test. Knowing the physical length of line, l_e, and the approximate effective dielectric constant (from Wheeler), the approximate distance which the reference node had moved towards the load could be calculated. The exact position of the minimum was then located using the technique described previously, and the nodal shift, l_o, could then be measured. As the shift was greater than the range of the micrometer adjustment, highest accuracy was obtained using vernier calipers, which were accurate to $\pm$ 0.005mm. Therefore, overall accuracy of measurement of the shift of the node was $\pm$ 0.27mm.

A plot of nodal shift versus frequency was constructed using the above procedure, and is shown in figure 3.9.

A line AA' is drawn on the graph such that the intercepts on the X axis of the nodal shift plot are equal. At these points, $\frac{\beta_o l_o}{\beta_e l_e} = 1$, and the effective dielectric constant can be found using equation 3.10.

Using this equation, the value of E_{eff} could be determined at each of the cross-over points (i.e. throughout X band), and the resulting values are given in section 3.5.

The microstrip line characteristic impedance is determined using equation 3.13. The frequency at each of the peaks is determined from the plot, and the value of $\beta_o l_o$ can then be determined using the measured value of nodal shift at that point.

The ratio of $\frac{\beta_o l_o}{\beta_e l_e}$ is determined from the ratio of peak nodal shift at each of the maxima in turn, and hence the value of Z_e at each of these frequencies could be determined.

The results are tabulated and discussed in section 3.5.

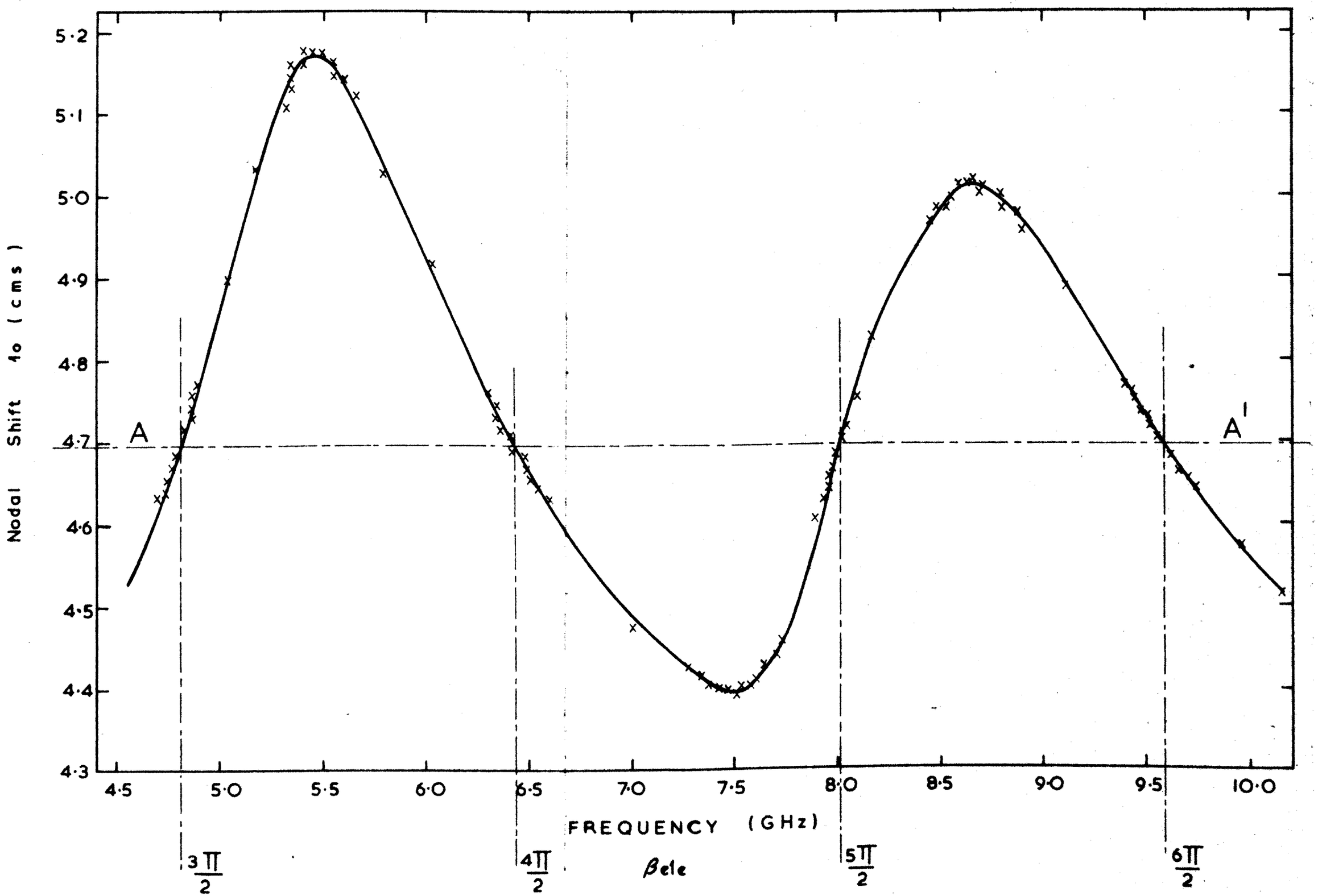
Figure 3·9

PLOT OF NODAL SHIFT (1o) versus FREQUENCY

Sample: A

Substrate: Quartz

Nominal Impedance: 18·6 ohms



3.4.4 Time domain reflectometry.

The samples used in the nodal shift technique were modified by the removal of the remaining short circuit, which was replaced by a matched load (APC-7 matched load, with APC-7 to microstrip transition, type OSM 14493A). The V.S.W.R. of the load was 1.1, which implies the impedance may vary from 45 to 55 ohms, which was of insufficient accuracy to act as a reference short circuit. A 10 cm section of 50 ohm air-line (HP 11566A) was therefore inserted before the test sample, and a 5 cm air-line between the test sample and the load to act as high precision reference impedances.

Measurements were then carried out on each of the lines in turn, using the Hewlett Packard 1415A T.D.R. unit, and the results are tabulated in section 3.5.

3.4.5 Theoretical methods.

Direct numerical methods can give the characteristic impedance to within 0.6%[123], but the analysis is not amenable to practical design situations without the use of a computer.

However, using the theory of Schneider[120], E_{eff} can be calculated to within 3%, and then using Schneider's earlier derivation of Z (equation 3.1-3.4), the characteristic impedance can be determined.

Alternatively, Jain's[121] theory (accurate to within 5%) may be used.

For comparison purposes only, the values of E_{eff} and Z, calculated from both Jain's and Schneider's analyses, are compared with measured data in section 3.5. As discussed earlier, they are of insufficient accuracy to be relied upon in isolation for the application discussed in this thesis.

3.5 Analysis of the results of measurements of microstrip lines on quartz substrates.

3.5.1 Results of E_{eff} determination.

The results of the dispersion measurements of various

impedance lines on quartz substrates, using the nodal shift technique and Mehmet's method, are tabulated in figure 3.10. A plot of effective dielectric constant versus frequency for these lines is given in figure 3.11. In this figure, Mehmet's method clearly shows the effect of dispersion. However, due to measurement inaccuracies using the nodal shift technique, the spread in results is greater than the amount of dispersion present, and therefore no indication is given by the nodal shift technique, of the degree of dispersion of microstrip lines on quartz substrates. So although measurements are made throughout X band, only an average value of E_{eff} can be obtained from these measurements, and no indication of dispersion can be deduced.

The maximum deviation between the two measurement techniques is 2.1%, and, on average, is approximately $\pm$ 0.8%, which is within the estimated accuracy of the measurement techniques (i.e. $\pm$ 0.2% for Mehmet's method (Appendix 3.3), and $\pm$ 1.5% for the nodal shift technique (Appendix 3.4)).

The general trends of the results agrees with those found by others[100,101,103,104], namely, that for a given substrate, dispersion increases for decreasing impedance.

Assuming the variation in E_{eff} is directly proportional to frequency for a given microstrip line at X band, as has been shown[104] to be the case, then the results can be normalised to standard frequencies of, say, 10 GHz and 7 GHz. Then, by linear interpolation, the value of E_{eff} at any intermediate frequency can be determined. This procedure is adopted in figure 3.12, in which the effective dielectric constant, at frequencies of 10 GHz and 7 GHz, is plotted as a function of $\frac{w}{h}$.

This figure indicates a deviation from the T.E.M. solution of the effective dielectric constant of 1.3% for Z_o = 65 ohms, and 3.6% for Z_o = 20 ohms. Comparing these values with published data for other substrate materials[101-104], general agreement is observed with Deutsch's[104] conclusion that dispersion decreases for a decrease in substrate dielectric constant.

MEASUREMENTS OF EFFECTIVE DIELECTRIC CONSTANT

Substrate : Quartz Dielectric constant : 3·78 Substrate thickness : 0·5 m.m.

MICROSTRIP PHYSICAL PROPERTIES						RESONATOR METHOD			NODAL SHIFT METHOD			
Sample	Line Width m.m.	Line Length m.m.	Substrate thickness m.m.	$\frac{w}{h}$	Nominal Z_o Schneider	Resonant frequency GHz	Mode n	Effective dielectric constant E_{eff}	Frequency GHz	Mode m	Effective dielectric constant E_{eff}	Sample
A	4·044	25·165	0·489	8·27	18·63	6·433157	2	3·434	4·81	3	3·45	A
									6·40	4	3·47	
						9·606473	3	3·465	8·01	5	3·46	
									9·57	6	3·49	
B	2·851	24·783	0·499	5·7	25·11	6·609276	2	3·301	5·02	3	3·27	B
									6·65	4	3·31	
						9·870651	3	3·33	8·33	5	3·3	
									9·85	6	3·4	
C	1·581	24·522	0·513	3·08	39·5	6·919439	2	3·126				C
						10·347759	3	3·145				
D	1·466	24·972	0·502	2·9	41·44	6·817688	2	3·105				D
						10·197018	3	3·123				
E	1·211	24·993	0·492	2·46	45·81	6·873104	2	3·05				E
						10·291116	3	3·061				
F	0·873	24·956	0·480	1·82	54·92	6·968348	2	2·976				F
						10·436752	3	2·985				
G	0·721	25·128	0·516	1·4	63·39	7·286253	2	2·912				G
						10·914397	3	2·92				

Figure 3·10

Figure 3·11

EFFECTIVE DIELECTRIC CONSTANT

v

FREQUENCY

Experimental results

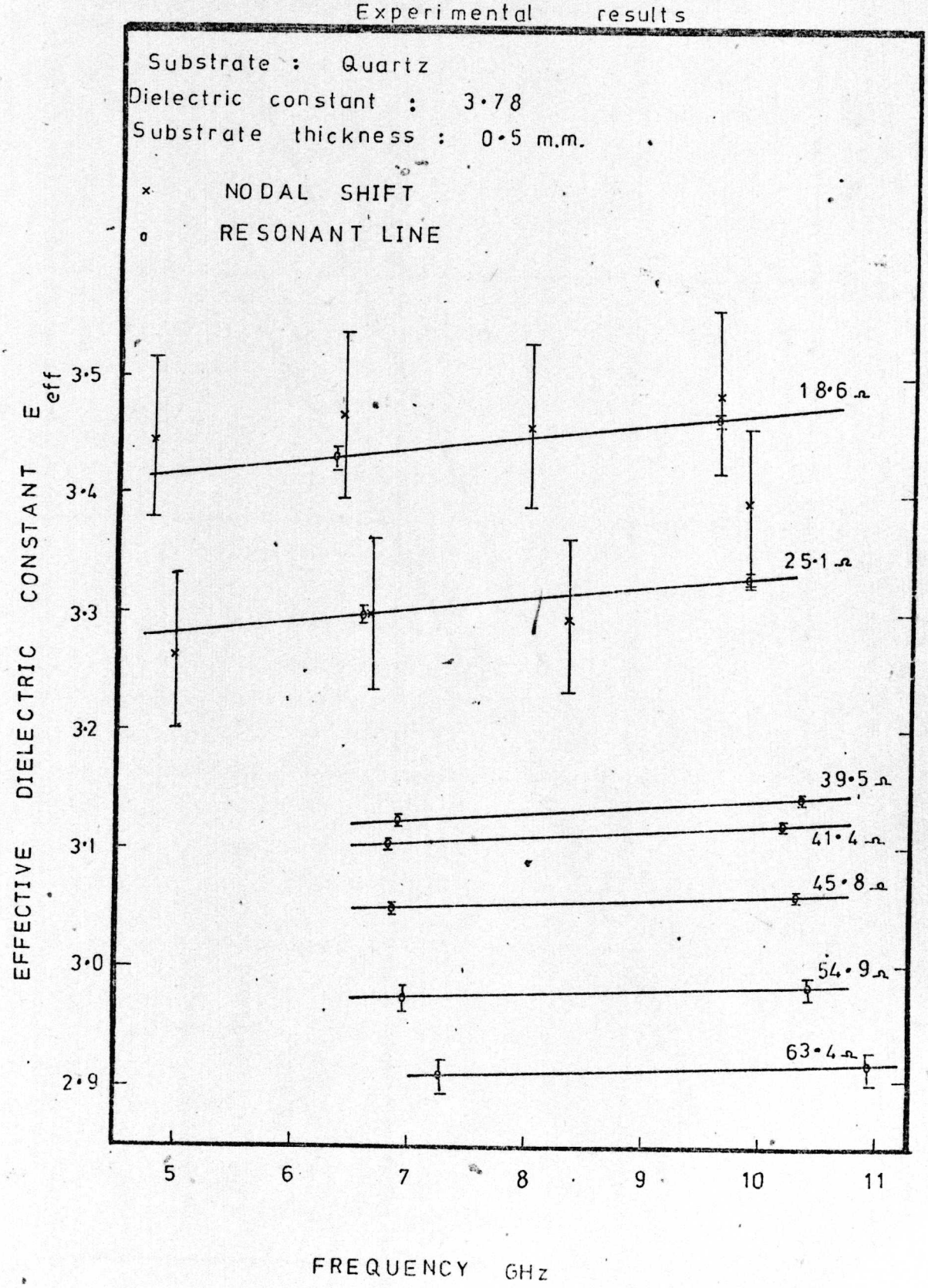


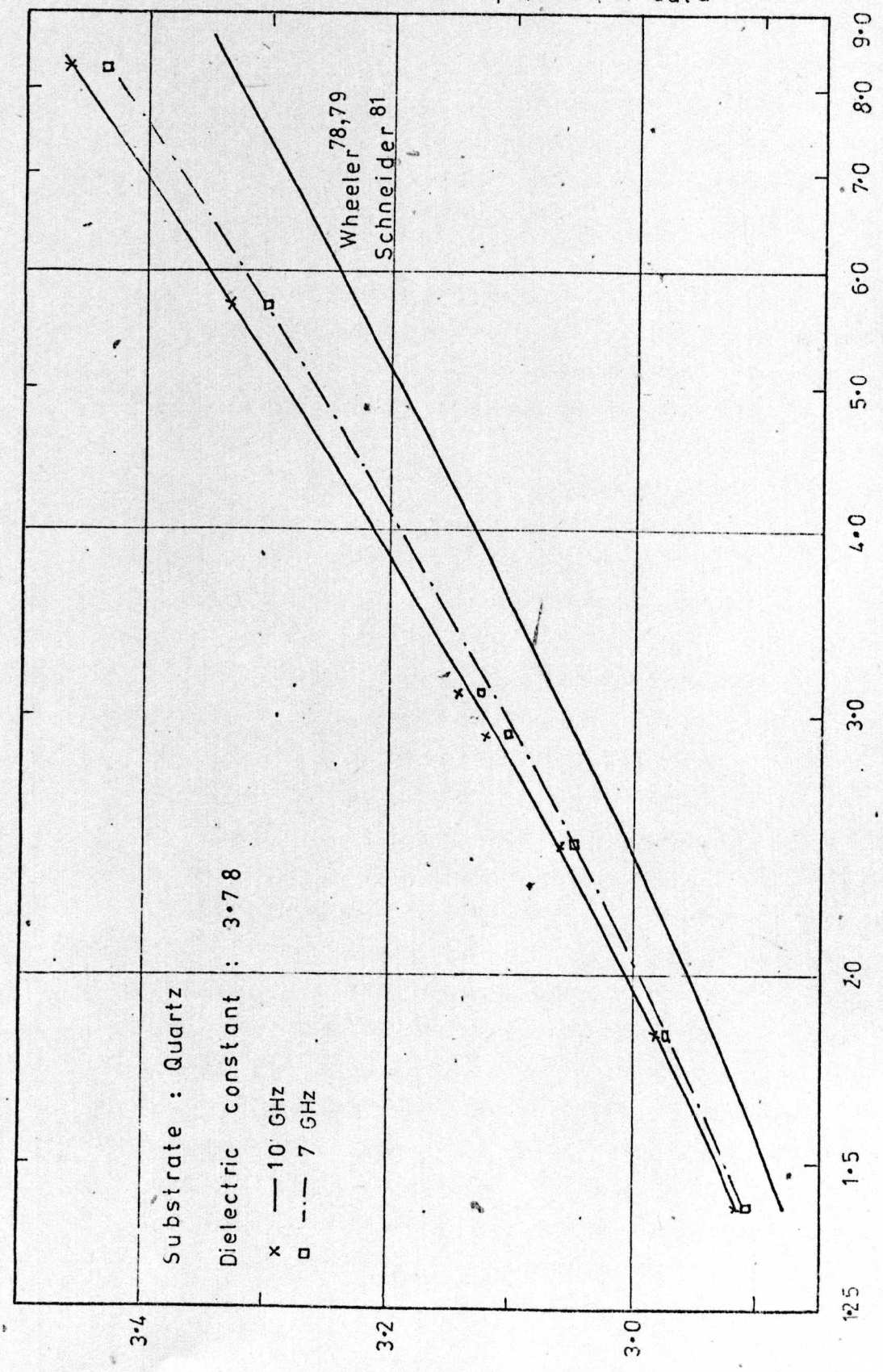
Figure 3·12

EFFECTIVE DIELECTRIC CONSTANT

v

LINE WIDTH
SUBSTRATE THICKNESS

Interpolated results from experimental data



The only published data available for E_{eff} of microstrip lines on quartz, are due to Van Nie[124] and Mehmet[19]. Van Nie reported no dispersion for 50 ohm lines within the accuracy of his measurement technique (3%). Mehmet's measurements, and those carried out by the author, indicate dispersion of less than 3% for 50 ohm lines, which consequently would not be evident in Van Nie's measurements. Mehmet quotes only one result for quartz, which is 0.67% lower than the author's measured values, although the same resonant technique has been adopted. This discrepancy is most probably due to the rounded edges of the substrate which Mehmet has not accounted for, and which can lead to errors of up to 1% in E_{eff}, as described in section 3.4.2.

Comparison of results obtained by the author, with later, more accurate measurements by Van Nie[125] (in which he admits that dispersion is evident), shows agreement to within $\pm$ 0.5% for $1 \leq \frac{w}{h} \leq 10$. No accuracy is quoted by Van Nie for these measurements.

In figure 3.13, some of the measured results obtained using Mehmet's method are compared with the theoretical results obtained from Schneider[120] and Jain[121], Also, for comparison purposes, the T.E.M. solution of Schneider[81] is included. From this figure it can be seen that Jain's theory approximates the experimentally obtained values more closely than does Schneider's dispersion theory. For low impedance lines (i.e. 18 ohms) at 5 GHz, the theoretical values of Jain and Schneider are approximately 2.5% lower than the measured values, and at 12 GHz, this decreases to 1% for Jain's theory, and increases to 5% for Schneider's dispersion theory. For high impedance lines, both theoretical analyses underestimate the measured values of E_{eff} by approximately 1% at 5 GHz, whereas at 12 GHz, Jain's theory is 0.7% lower, and Schneider's is 1.25% lower, than the measured values.

Schneider claims 3% accuracy for 50 ohm lines on alumina substrates, and it appears that this theory is accurate to within these limits for reasonably high impedance lines on quartz substrates. For low impedance lines (less than 25 ohms), the accuracy is slightly lower, as indicated above.

For Jain's theory, the results are claimed to be

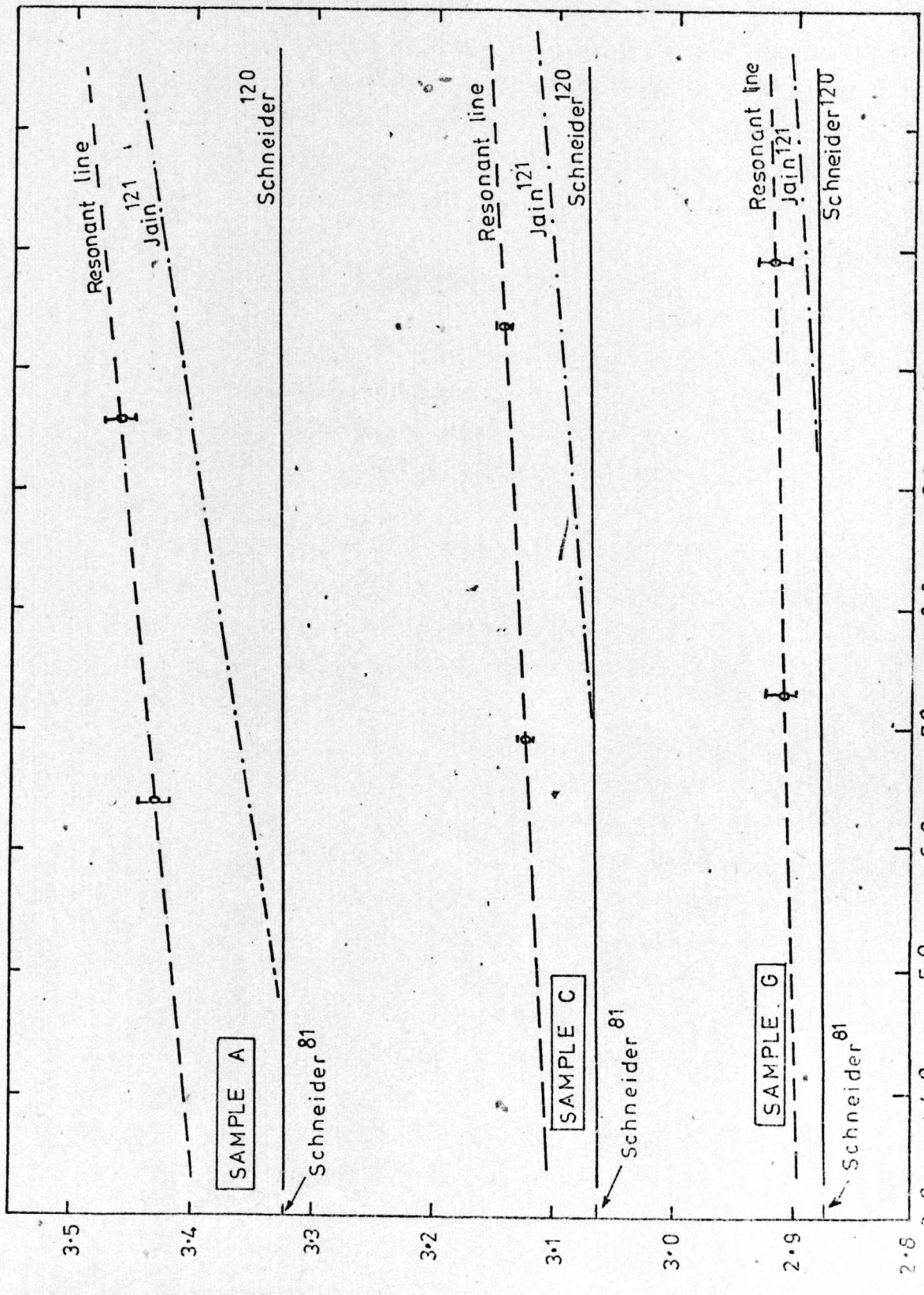
Figure 3·13

EFFECTIVE DIELECTRIC CONSTANT

v

FREQUENCY

Comparison of experimental and theoretical results



accurate to within 5% if $2 \leq e_r \leq 104$; $0.025" \leq h \leq 0.125"$; $0.9 \leq \frac{w}{h} \leq 6$.

Although the tested substrates fall outside these limits (h=0.020"), the measured results are well within the specified limits of accuracy, notedly so for high impedance lines at the higher microwave frequencies.

It appears, therefore, that results derived from Jain's theory agree with the measured data to a higher degree of accuracy than results derived using Schneider's theory; and using Jain's analysis, the agreement is within 1% for all measured lines at 12 GHz. It appears, therefore, that Jain's analysis will be extremely useful in practical design cases where measured values of E_{eff} are not available.

3.5.2 Results of impedance evaluation.

The results of the measurements of the characteristic impedance of microstrip lines on quartz substrates using the techniques described in section 3.4 are tabulated in figure 3.14, and in figure 3.15, a plot of impedance, Z, against $\frac{w}{h}$ is also given.

As discussed previously, using the nodal shift technique, no indication of dispersion can be deduced as the amount of dispersion is less than the accuracy of the measurements. Agreement with the results of Mehmet's method, however, is within 6%.

In figure 3.16, the results of Mehmet's method are compared with the T.E.M. solution and the theories of Jain and Schneider. The results of Mehmet's technique clearly show the dispersion effects, and for low impedance lines (i.e. 18 ohms), the impedance at 10 GHz is 1.5% lower than the T.E.M. solution, and for high impedance lines (i.e. 63 ohms) at the same frequency, the impedance is 0.67% lower than the corresponding T.E.M. solution. The results obtained from the T.D.R. measurements agree to within 0.7% with the T.E.M. solution of Wheeler.

As discussed previously, the results obtained from Schneider's theoretical analysis appear to be less accurate than those derived from Jain's theory.

Substrate	$\frac{w}{h}$	CHARACTERISTIC IMPEDANCE (ohms)						
		[81] Schneider Ω	T.D.R. Ω	Nodal Shift		Resonator		
				Frequency GHz	Impedance	Frequency GHz	E_{eff}	Impedance
A	8·27	18·63	18·5	5·44	20·66	6·433	3·434	18·35
				7·47	17·34	9·606	3·465	18·25
				8·645	20·61			
B	5·7	25·11	25·0	5·35	26·52	6·609	3·301	24·83
				7·357	22·74	9·87	3·33	24·72
				8·523	26·24			
C	3·08	39·5	39·2			6·919	3·126	38·11
						10·348	3·145	39·0
D	2·9	41·44	41·0			6·818	3·105	40·77
						10·197	3·123	40·65
E	2·46	45·81	45·76			6·87	3·05	45·49
						10·29	3·061	45·41
F	1·82	54·92	54·81			6·958	2·976	54·54
						10·437	2·985	54·46
G	1·4	63·39	63·33			7·286	2·912	63·01
						10·914	2·92	62·92

Figure 3·14 Results of impedance measurements of microstrip lines on quartz substrates

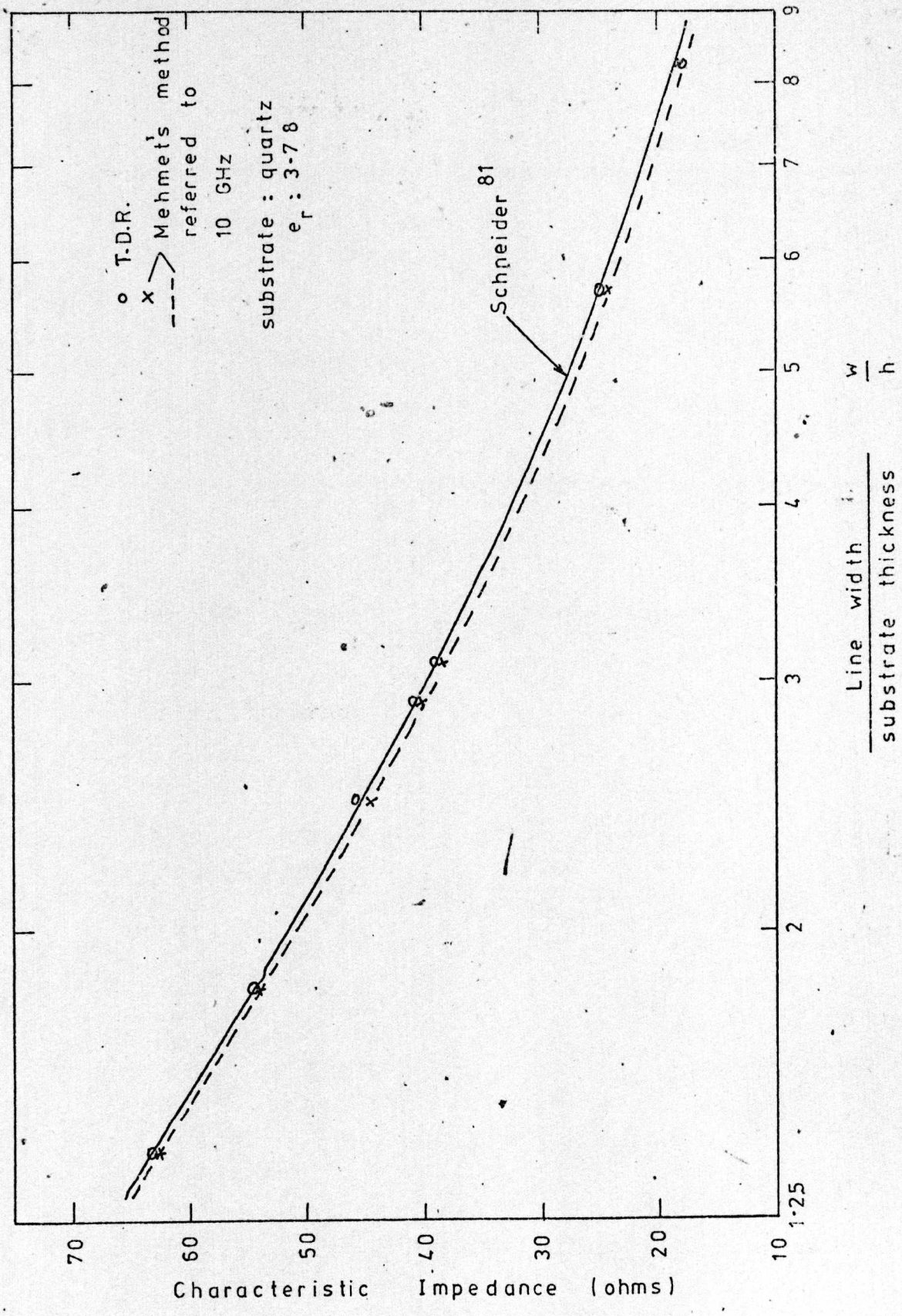
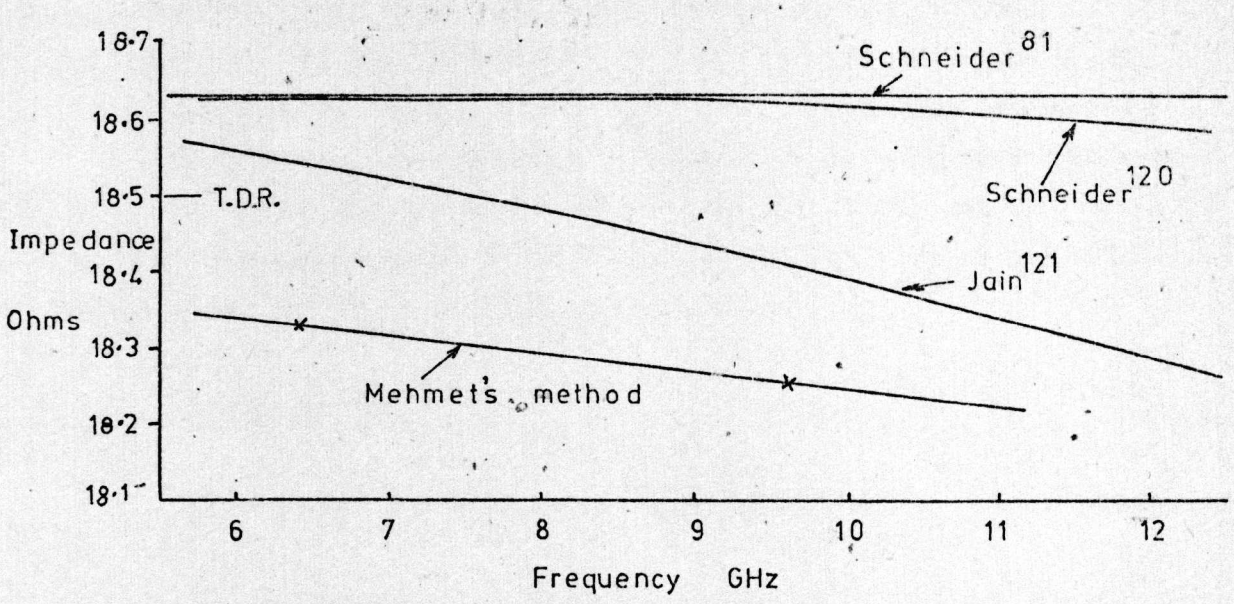
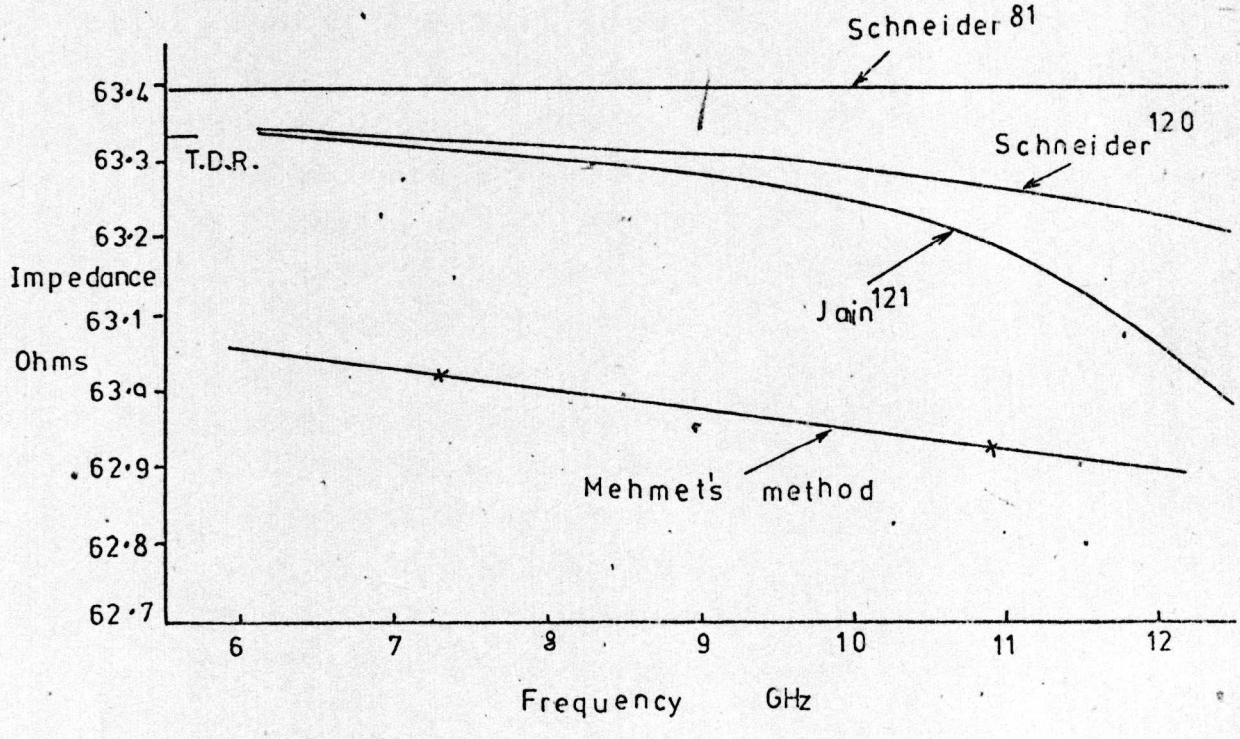


Figure 3·15 Characteristic Impedance as a function of $\frac{w}{h}$.



(a) Low frequency impedance 18·63 ohms



(b) Low frequency impedance 63·3 ohms

Figure 3·16 Impedance as a function of frequency

Jain's theory predicts the impedance to within approximately 0.75% for low impedance lines at 10 GHz (compared with 2% for Wheeler's T.E.M. analysis), and 0.5% for high impedance lines (compared with 0.75% for Wheeler).

Therefore, as indicated previously, the theoretical analysis of Jain can be used as a valuable tool in the evaluation of the impedance of microstrip lines, where practical measured data of E_{eff} is not available.

3.6 Conclusions.

The major conclusions to be drawn from this chapter are;

1. at the outset of the project, the most accurate method available to the author for determining the transmission characteristics of microstrip lines, was to measure the effective dielectric constant using Mehmet's method, and then to calculate β and Z using equations 3.1 - 3.4. The accuracy of calculation of β is then better than $\pm$ 0.1%, and for the impedance, Z, is better than $\pm$ 0.35%. $(0 \leq \frac{w}{h} \leq 10)$.
2. for microstrip lines on quartz substrates, a general plot of characteristic impedance as a function of $\frac{w}{h}$ is given in figure 3.15.
3. the value of E_{eff} for quartz substrates, for any $\frac{w}{h}$ is given by figure 3.12, for the frequencies of 7 GHz and 10 GHz. The value of E_{eff} for any other frequency can then be found by linear interpolation.
4. if a theoretical derivation of E_{eff} is required, Jain's theory should be used in preference to Schneider's, and at 10 GHz, the value derived by Jain's theory is approximately 1% lower than the practically measured results, for $18 \leq Z_o \leq 65$.

The practical measurement results obtained in this chapter, are used extensively throughout the remainder of the thesis, and are a basis for the design and characterisation of the microstrip circuits used in this project. In particular, the results have most significance in the design and operation of the measurement technique devised to investigate the properties of thin film overlay capacitors discussed in chapter 5.

4. MICROSTRIP DISCONTINUITIES.

4.1 Introduction.

In the preceding chapter, the transmission characteristics of microstrip lines on quartz substrates were investigated, to permit the accurate design and characterisation of the circuits used in the measurement of thin film capacitors.

As will become evident in Chapter 5, to allow accurate measurements of L.E's using the technique described, it is necessary to accurately evaluate the characteristics of 2 types of microstrip discontinuities. These are

1. gap discontinuity (figure 4.1)
2. gap-and-step discontinuity (figure 4.2).

In this chapter, therefore, the characteristics of these microstrip discontinuities wil be investigated. The extent to which the discontinuity characteristics are varied during the measurements, is governed by the data required to accurately design and operate the measurement technique for L.E. capacitors.

Although considerable published information exists concerning discontinuity characteristics in coaxial line[126,127] and strip line[128-132], no theoretical evaluation, and very little practical data was available at the outset of the project concerning the discontinuities in microstrip. In most applications, the theory of Oliner[128] for strip line is applied to microstrip discontinuities, but, as has been shown by James[133] for the gap discontinuity on alumina substrates, the deviation between the measured data, and the theoretical values derived from Oliner, is not less than 10%. Therefore Oliner's theory was not considered further as an accurate means of determining the discontinuity characteristics for this project.

Where practical data was available[133,134], it referred to discontinuities on alumina substrates, and therefore was not applicable in this case where quartz substrates are used. Therefore, all data required for this project had to be

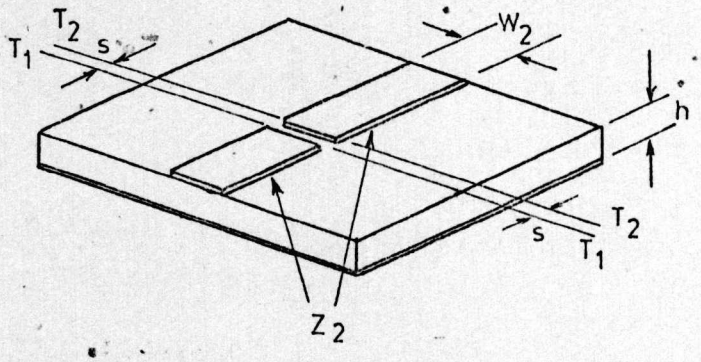


Figure 4·1 Gap discontinuity

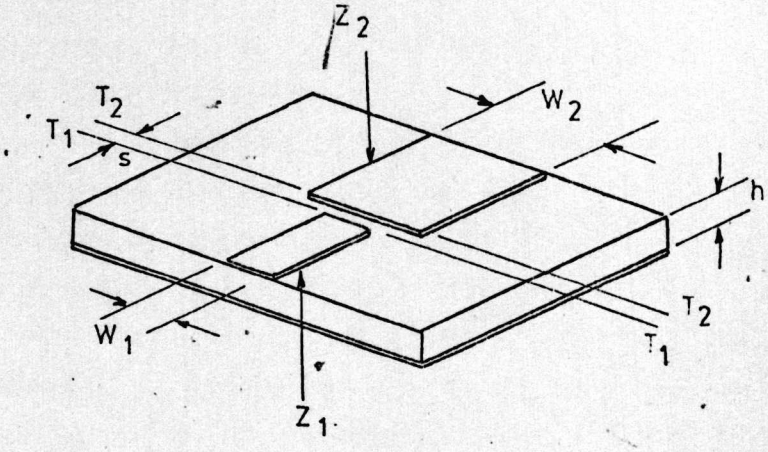


Figure 4·2 Gap-and-step discontinuity

determined by practical methods, and by techniques developed predominantly by the author.

At a later stage in the project, significant published data[135-139] did become available regarding the theoretical evaluation of some of the microstrip discontinuity characteristics, and where relevant, these theoretical predictions have been compared with the data measured by the author.

The measured results obtained in this chapter will provide valuable data for the design of the measurement technique for lumped element capacitors, described in Chapter 5.

4.2 General measurement technique for microstrip discontinuity characteristics.

A microstrip resonator, short-circuited at both ends, has been shown (sect. 3.4.2) to be an extremely valuable measurement tool, as it allows high measurement accuracy but with a resonator of simple design and construction. In this chapter, a short-circuited resonator is used to accurately determine the characteristics of the two microstrip discontinuities under investigation.

The lowest order resonant modes of a resonator short-circuited at both ends, are shown in figure 4.3. From this figure, it can be seen that the midpoint of the resonator is either a point of maximum voltage and zero current (i.e. nodes n = 1,3 etc,), or a point of maximum current and zero voltage (i.e. nodes n = 2,4 etc.) If a lumped series element were to be introduced at the midpoint of the resonator, for the odd half-wavelength modes (i.e. n = 1, 3 etc), the voltage on both sides of the series component would be equal (due to the symmetrical nature of the voltage waveform). No current would therefore flow through the element, and no perturbation of the resonator frequency, or Q factor, would be observed. If, however, the even resonance modes were to be used (i.e. n = 2, 4 etc.), a voltage difference would exist across the component due to the finite component length, and the device would perturb both the resonant frequency and the Q factor of the line.

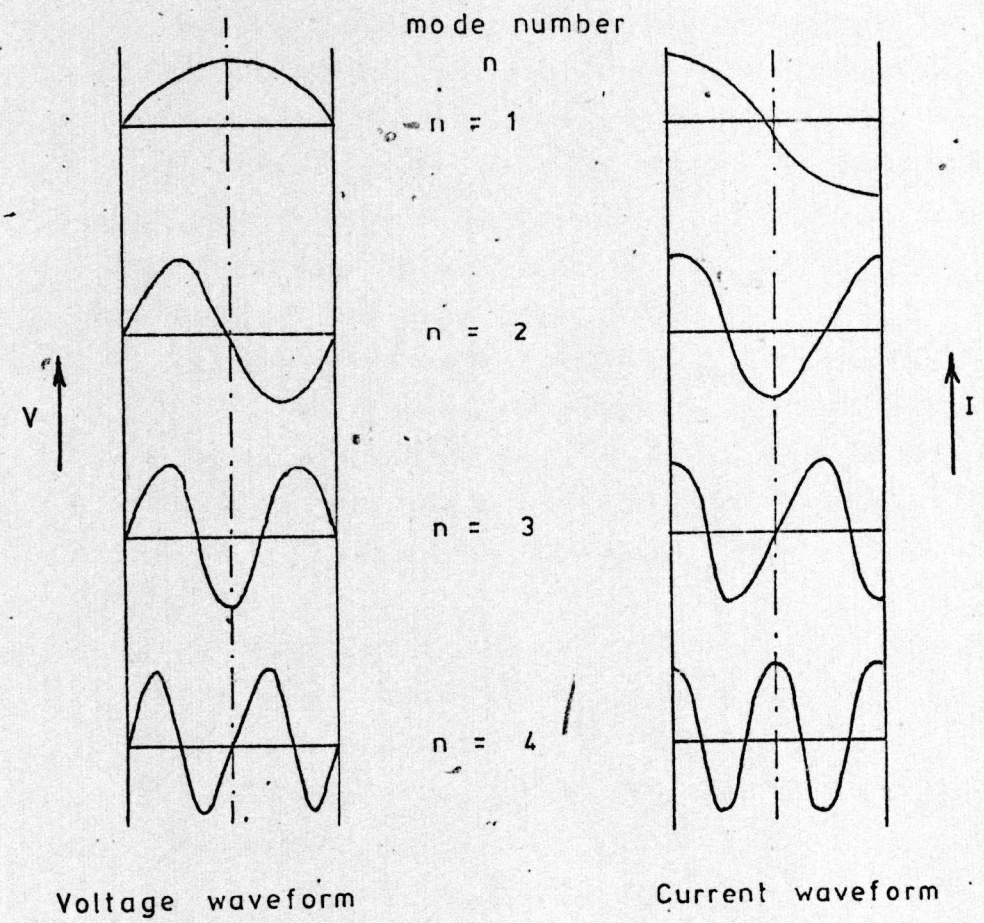


Figure 4·3 Voltage and current waveforms for the lowest order modes of a resonant line short-circuited at both ends.

If, on the other hand, a shunt element were to be introduced at the midpoint of the resonator, the odd modes would produce the maximum voltage across the element, and, therefore, maximum perturbation of the microstrip resonator properties would be experienced. If the even modes were to be used, the voltage across the element would be zero, and no perturbation would, therefore, result.

If a component, whose characteristics are to be measured, is introduced at the centre of a perfectly symmetrical resonator, short circuited at both ends, the series characteristics of the element can be ascertained by taking measurements at the frequencies of even-mode resonances, and the shunt characteristics by taking measurements at the frequencies of odd-mode resonances.

Apart from the advantages mentioned previously (section 3.4.2), of the simple resonator construction, a further advantage of the technique is that because of the symmetrical nature of the resonator, the theoretical analysis required to extract the desired component characteristics, is extremely simple.

This technique, therefore, was adopted for the measurement of the two discontinuities under investigation. The theory and practical experimental details relative to each of the discontinuities, will be discussed in detail in the following sections.

4.3 Gap discontinuity.

The equivalent circuit of the gap discontinuity[136] (figure 4.1), is given in figure 4.4. For the purposes of this investigation, the line impedances on either side of the gap are assumed to be constant at 32 ohms, and the gap width, s, is varied from approximately 5 μm to 100 μm ($0.01 \leq \frac{s}{h} \leq 0.2$).

4.3.1 Measurement technique.

As discussed previously, the measurement technique adopted utilises a linear resonant line, short circuited at both ends, with the gap discontinuity located at the midpoint of the line. A schematic of the resonator is given in figure 4.5, and the equivalent circuit is given in figure

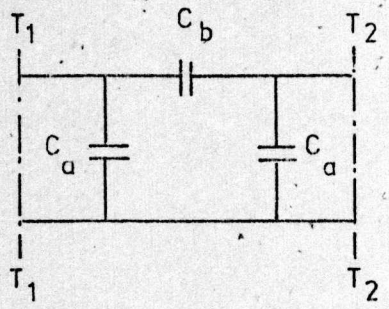


Figure 4·4 Equivalent circuit of a gap in microstrip (edge representation)

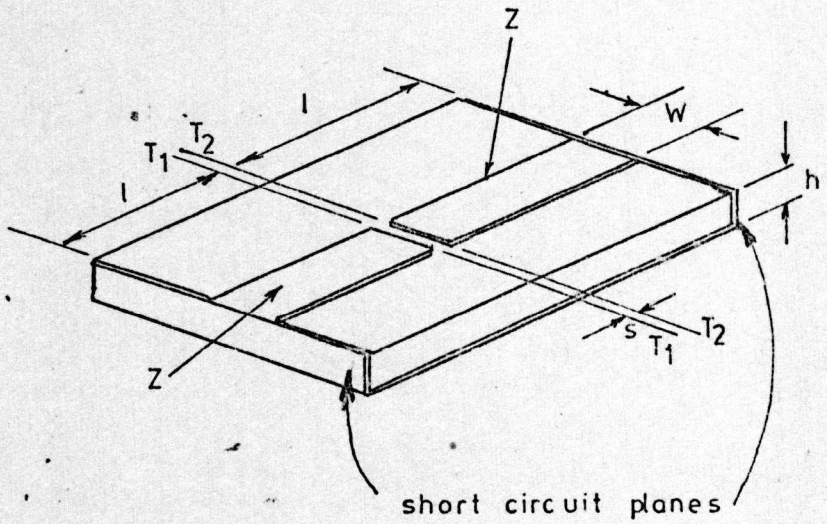


Figure 4·5 Schematic diagram of resonator used for measuring the gap capacitance

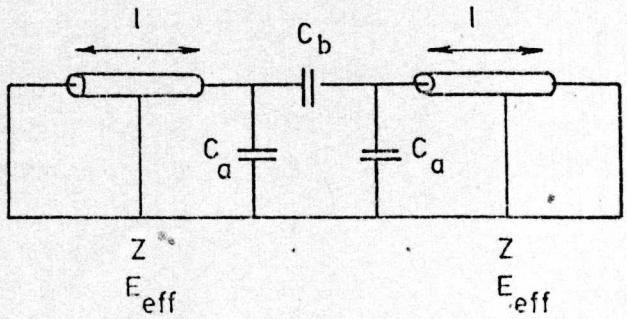


Figure 4·6 Equivalent circuit of the resonator of figure 4·5

4.6. The possible lowest order modes of the resonator (for $0 \leq C_b \leq \infty$, and $C_a \rightarrow 0$), are shown in figure 4.7.

Determination of the shunt capacitance, C_a.

If the resonant frequency is selected such that the voltages on both sides of the series capacitor, C_b, are equal, (i.e. mode n = 1,3 etc.), then no current will flow through the capacitor, C_b, (figure 4.8), and the gap equivalent circuit can be reduced to that shown in figure 4.9. The resulting equivalent circuit of the complete resonator is then shown in figure 4.10. The conditions at resonance (Appendix 4.1), are then

$$C_a = \frac{1}{\omega Z} \cot \frac{\omega l \sqrt{E_{eff}}}{c} \qquad 4.1$$

Therefore, if the resonant frequency is chosen such that the voltage is the same on both sides of the discontinuity, (i.e. n = 1, 3 etc.), the shunt capacitance, C_a, can be determined.

Determination of the series capacitance, C_b.

The π equivalent circuit of the microstrip gap (figure 4.4), can be transformed to an equivalent T circuit (figure 4.11) using the transformation identity derived in Appendix 4.2. Using this equivalent circuit for the gap, it can be seen that for the resonant modes where the voltage to ground at the midpoint of the gap is zero (i.e. modes n = 1A, 2, 3A figure 4.7), then the voltage across the shunt capacitance, $C_a(2 + \frac{Ca}{Cb})$, (figure 4.12), is zero, and no current flows through this capacitor. The gap equivalent circuit can then be reduced to a single series capacitance, $C_b + \frac{C}{2}a$, (figure 4.13), and the complete test resonator equivalent circuit can be reduced to that shown in figure 4.14. The resulting resonant conditions can be shown (Appendix 4.3) to be

$$C_b + \frac{C_a}{2} = \frac{1}{2\omega Z \tan \beta l} \qquad 4.2$$

Therefore, if the resonant frequency is arranged so that modes 1A, 2, 3A etc. are used, then the capacitance $C_b + \frac{Ca}{2}$, can be determined. Then, having calculated C_a

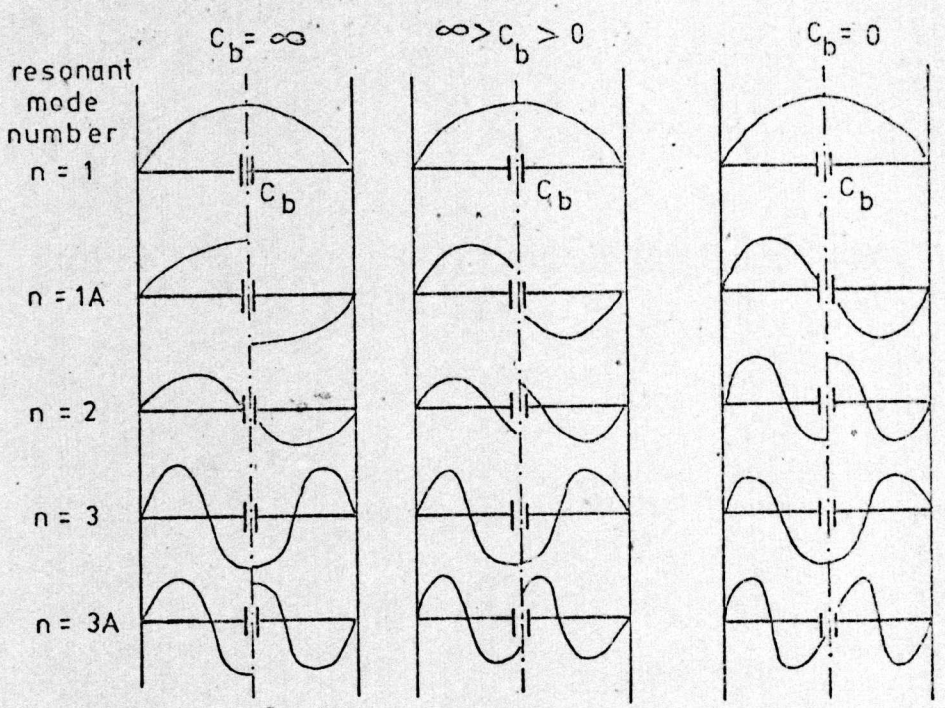


Figure 4·7 Voltage mode diagrams for microstrip resonators with a capacitive gap (figure 4·5)

($C_a = 0$, $0 < C_b < \infty$)

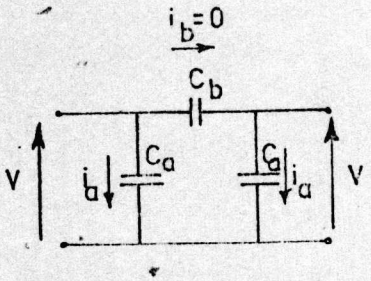


Figure 4·8 Voltage and current conditions for modes n = 1,3 etc.

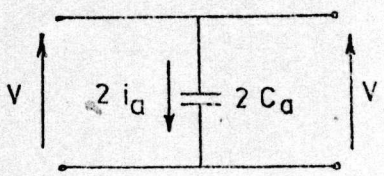


Figure 4·9 Simplified circuit of figure 4·3

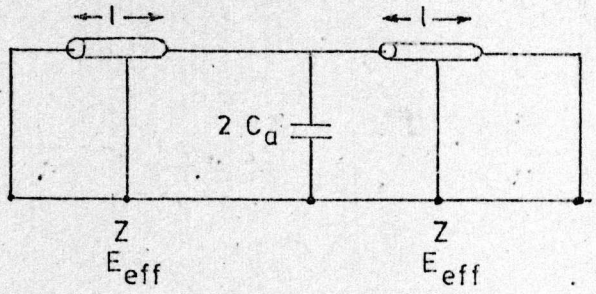


Figure 4·10 Resonator equivalent circuit for odd modes (n = 1, 3 etc)

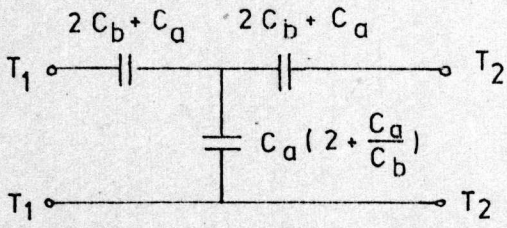


Figure 4·11 T equivalent circuit for a microstrip gap

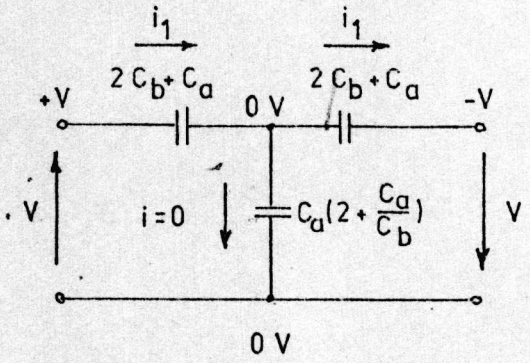


Figure 4·12 Voltage and current conditions for modes n=1A, 2, 3A etc.

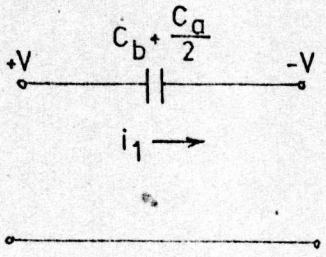


Figure 4·13 Simplified circuit of figure 4·12.

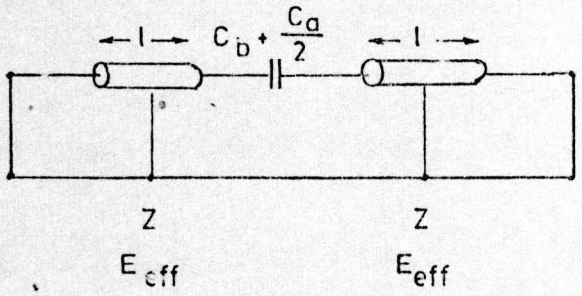


Figure 4·14 Resonator equivalent circuit for modes n = 1A, 2, 3A etc.

from the preceding measurement, and assuming that the change in C_a due to the difference in frequencies between the two measurements, is negligible, the gap series capacitance, C_b, can be determined. Therefore, from the two measurements at two different frequencies, using the same resonator, the characteristics of the microstrip gap can be fully determined.

4.3.2 Fabrication of the resonator samples.

The X band resonators were constructed on 1"x1"x0.020" quartz substrates, using the technique described in Appendix 4.4. Considerable effort was employed in devising a process which produced uniform gap widths, good edge definition, high yields, high Q factors, and with the minimum of processing stages. The process adopted has proved to be the most satisfactory technique so far used by the author for this type of circuit.

All test samples had a nominal characteristic impedance of 32 ohms, and the gap width was varied from 5 μm to 100 μm.

4.3.3 Measurement procedure.

The test samples were enclosed in a brass shielding box (figure 5.27) to increase the resonator Q factor, and thus improve the measurement accuracy of the resonant frequency. Electrical connection to the line was made with an APC-7 to microstrip transition, with the body of the connector shorting the fringing fields. At the other end of the line, the fringing fields were shorted by an adjustable brass block, which was mounted in contact with the short circuit plane.

The frequencies of the two appropriate resonant modes were measured, by the technique described in section 3.4.2, using the X band coaxial reflectometer, shown in figure 3.3.

Using the measured physical dimensions of the resonators, the effective dielectric constants and the characteristic impedances of the microstrip lines, at the measured resonant frequencies, were then calculated by interpolation of the measured data of figure 3.12.

Hence, the capacitances, C_a and C_b, were determined using equations 4.1 and 4.2

4.3.4 Gap discontinuity results.

The results of the gap discontinuity measurements are tabulated in figure 4.15, and graphs of the shunt capacitance, C_a, and the series capacitance, C_b, as a function of the ratio of gap width to substrate thickness, are given in figures 4.16 and 4.17 respectively.

For a gap width to substrate thickness ratio of 0.1, the measurement accuracy (Appendix 4.5) is approximately $\pm$ 60% for the shunt capacitance, C_a, and $\pm$ 3% for the series capacitance, C_b.

The accuracy of measurement of C_a is therefore considerably less than that of C_b, and if more accurate values for C_a are required, a more precise measurement technique would have to be devised.

In figure 4.16 and 4.17, the measured data is compared with results derived from the theoretical analysis of Oliner[128], and also from values interpolated from theoretical graphs of Maeda[135] and Farrar[136]. In the case of the latter two, accuracy of the data is governed by the uncertainty of the interpolation from the published graphs.

Also shown in figure 4.17, for comparison purposes at this stage, are the results of measurements made at a later date in the project (Chapter 8), using a completely independent measurement technique.

The main observation to be made at this stage, from the results shown in figures 4.16 - 4.17, is that, for $\frac{s}{h}$ less than, or equal to, 0.1, the series capacitance, C_b, is at least 15 times greater than the shunt capacitance, C_a.

Comparing the theoretical predictions of Farrar, Maeda, and Oliner with the measured results, for the shunt capacitance, C_a, the theories of Maeda and Oliner agree to within the accuracy of measurement of the technique described, with Farrar's results appearing slightly low.

For the series capacitance, C_b, Maeda's predictions are approximately 10% higher, Farrar's 50% lower, and Oliner's 60% lower than the measured data for $\frac{s}{h} = 0.1$, and all the theoretical predictions lie well outside the measurement accuracy of the resonator technique (i.e. $\pm$ 3%).

FIGURE 4·15

MEASURED MICROSTRIP GAP DISCONTINUITY PROPERTIES

Substrate : quartz $e_r = 3·78$

Sample	h (mm)	W (mm)	$\frac{W}{h}$	l (mm)	s mm	$\frac{s}{h}$	$E_{eff\,1}$	Z_1 (Ω)	Resonant frequency GHz	C_a pF	$E_{eff\,2}$	Z_2 (Ω)	Resonant frequency GHz	C_b pF
A	0·516	2·10	4·07	12·56	0·080	0·155	3·222	32·0	9·93865	0·01	3·210	32·55	9·497752	0·057
B	0·508	2·08	4·10	12·56	0·071	0·14	3·225	31·82	9·94513	0·00718	3·215	32·30	9·476053	0·06
C	0·512	2·08	4·05	12·53	0·059	0·115	3·221	32·09	9·97357	0·0076	3·212	32·35	9·462429	0·065
D	0·503	2·07	4·12	12·50	0·050	0·099	3·226	31·71	10·00194	0·0047	3·214	32·09	9·446575	0·072
E	0·499	2·08	4·17	12·55	0·041	0·082	3·23	31·43	9·96539	0·0024	3·220	32·80	9·406872	0·07
F	0·509	2·09	4·10	12·58	0·029	0·057	3·225	31·81	9·940552	0·0045	3·213	31·30	9·361109	0·08
G	0·498	2·07	4·15	12·51	0·020	0·04	3·229	31·54	10·00247	0·0016	3·217	31·81	9·381521	0·082
H	0·511	2·09	4·10	12·55	0·011	0·021	3·225	31·83	9·97291	0·0017	3·212	32·32	9·301299	0·09

FIGURE 4·16

Measured properties of a microstrip gap on quartz substrates at X band

Gap shunt capacitance as a function of gap width to substrate thickness ratio $\frac{s}{h}$

Microstrip line impedance 32 ohms

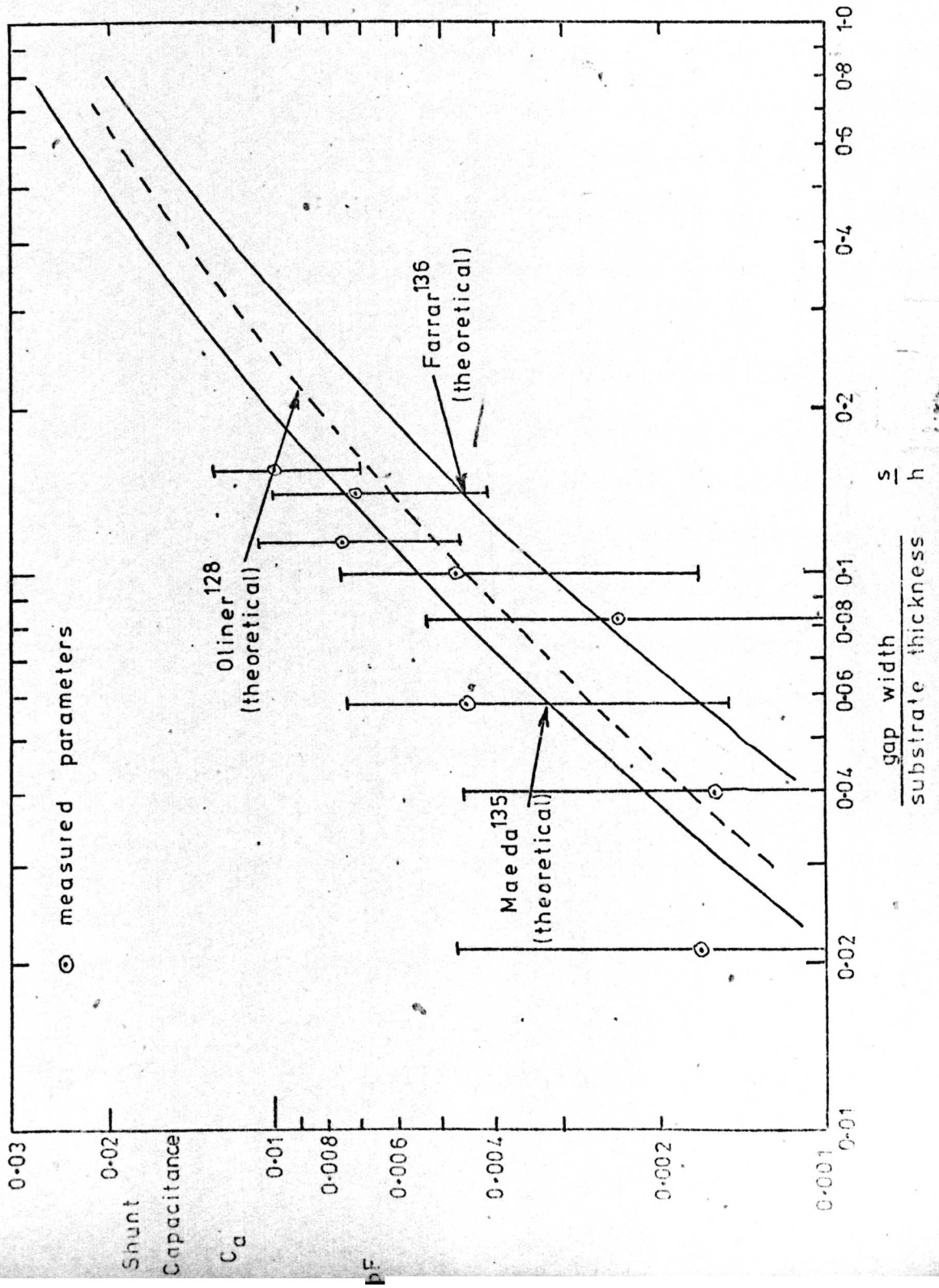
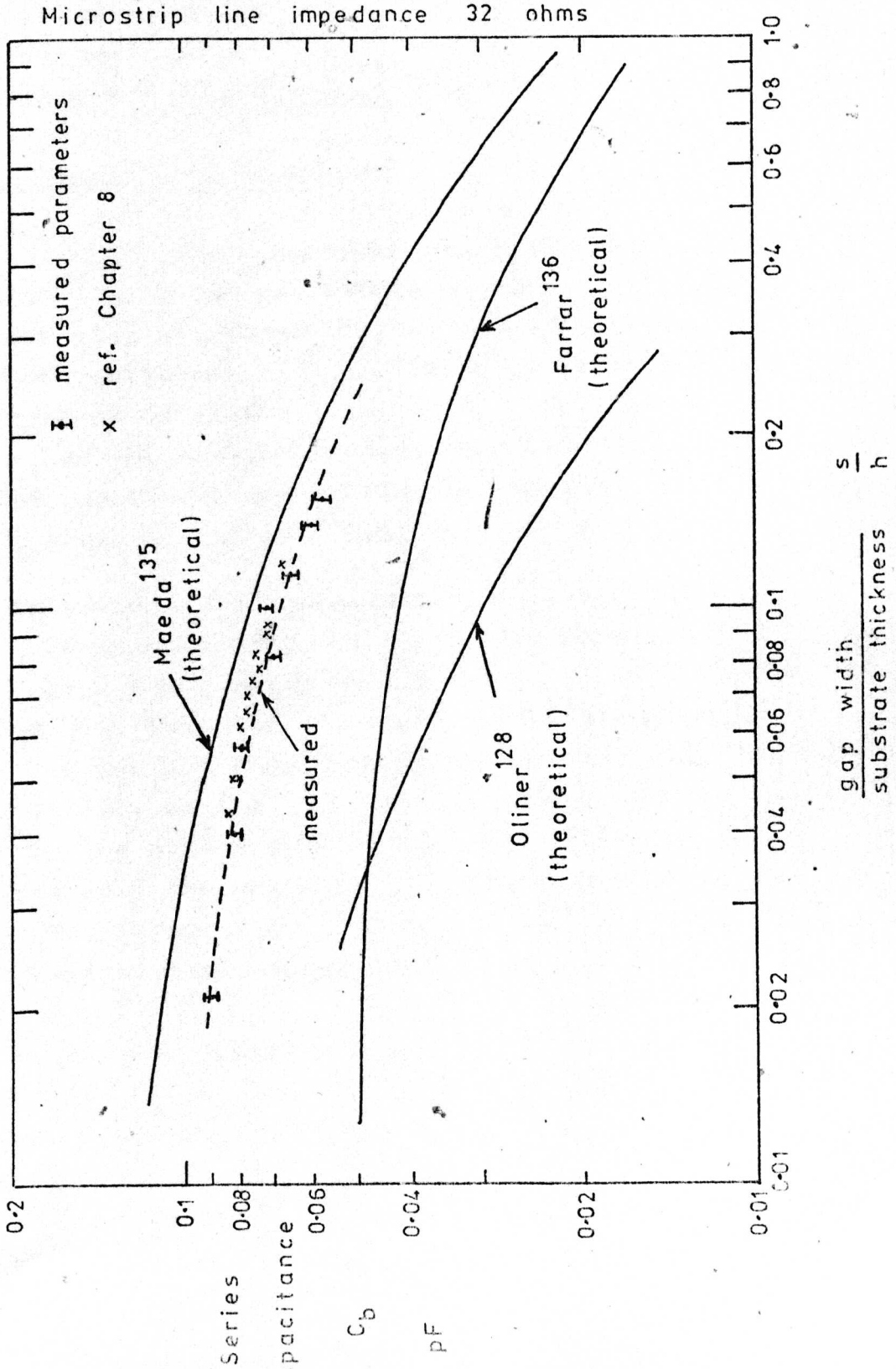


FIGURE 4-17

Measured properties of a microstrip gap on quartz substrates at X band

Gap series capacitance C_b as a function of gap width to substrate thickness ratio $\frac{s}{h}$

Microstrip line impedance 32 ohms



It would appear, therefore, that the results interpolated from Maeda's theory, predict the value of C_b to the greater degree of accuracy, but only to within 10%, and for future reference, this theory should be used in preference to either Oliner's or Farrar's. None of the theories, however, is considered to be of sufficient accuracy for the requirements of this project.

The data required in the design of the measurement technique for overlay capacitors is taken directly from figures 4.16 and 4.17.

4.4 Gap-and-step discontinuity.

4.4.1 Measurement technique.

A schematic diagram of the discontinuity, which is a combination of the microstrip gap discontinuity, and an impedance step discontinuity, is given in figure 4.2, and the exact equivalent circuit, which is derived in Appendix 4.6, is shown in figure 4.18.

For the particular discontinuity under investigation, the line impedances are maintained constant, with (figure 4.2) Z_1 = 50 ohms, and Z_2 = 32 ohms (i.e. $\frac{w}{w}1 \doteq 0.5$), and the gap width is varied from approximately 5 μm to 100 μm.

Using data obtained previously from the measurements of the gap discontinuity in isolation, it is shown in Appendix 4.6, that the exact equivalent circuit of the particular gap-and-step discontinuity under investigation (figure 4.18), can, to a first approximation, be represented simply by the series capacitance, C_c, of figure 4.19, providing that the gap width to substrate thickness ratio is less than approximately 0.1. If $\frac{s}{h}$ is greater than 0.1, the simplifications become less valid.

The test resonator used to measure the discontinuity capacitance, C_c, is a linear resonator, short circuited at both ends, and with the gap-and-step discontinuity located at the midpoint of the resonator (figure 4.20). The equivalent circuit is shown in figure 4.21, and the conditions for

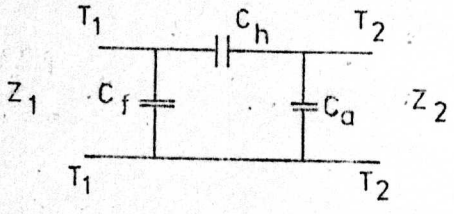


Figure 4·18 Equivalent circuit of the gap-and-step discontinuity

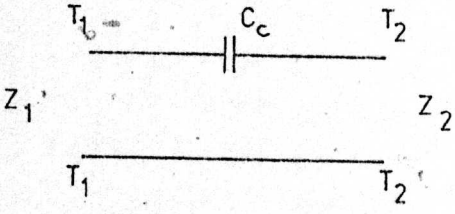


Figure 4·19 Simplified equivalent circuit of the gap-and-step discontinuity

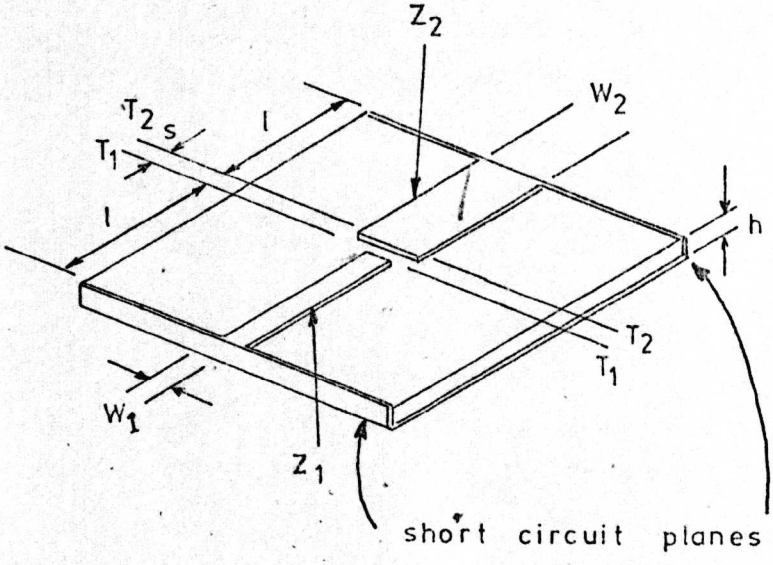


Figure 4·20 Test resonator for measuring the discontinuity capacitance C_c

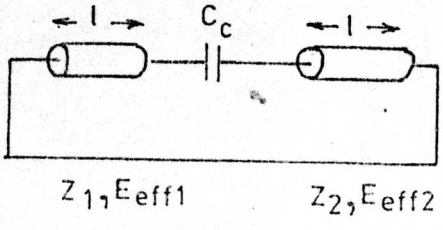


Figure 4·21 Equivalent circuit of test resonator

resonance are (Appendix 4.3)

$$C_c = \frac{1}{\omega} \frac{1}{Z_1 \tan\beta_1 l + Z_2 \tan\beta_2 l} \qquad 4.3$$

Therefore, by measuring the resonant frequency and the physical properties of the line, the capacitance, C_c, can be determined.

4.4.2 Design of the resonators

Several X band test samples were fabricated on quartz substrates using the process described in Appendix 4.4. All samples had fixed line impedances of Z_1 = 50 ohms, and Z_2 = 32 ohms, and microstrip gap widths varying from 5 μm to 100 μm.

4.4.3 Measurement procedure.

The measurements were performed at approximately 9.6 GHz, and the technique is similar to that described in section 4.3.3, and will not, therefore, be repeated at this stage.

4.4.4 Gap-and-step discontinuity results.

The measurement results are tabulated in figure 4.22 and a graph of the measured gap capacitance, C_c, as a function of the gap width to substrate thickness $(\frac{s}{h})$, is given in figure 4.23. The accuracy of the measurements has been shown (Appendix 4.7) to be approximately $\pm$ 2.7%.

The results are compared with theoretical values of microstrip gaps in 32 ohm lines and 50 ohm lines, obtained by interpolation from the graphs of Maeda[135]. The results are also compared with measured data obtained at a later stage in the project using a completely independent technique which will be discussed in Chapter 8.

The data required for the design of the measurement technique for overlay capacitors is taken directly from figure 4.23.

FIGURE 4·22

Measured microstrip gap-and-step discontinuity results

substrates : quartz ; dielectric constant = 3·78

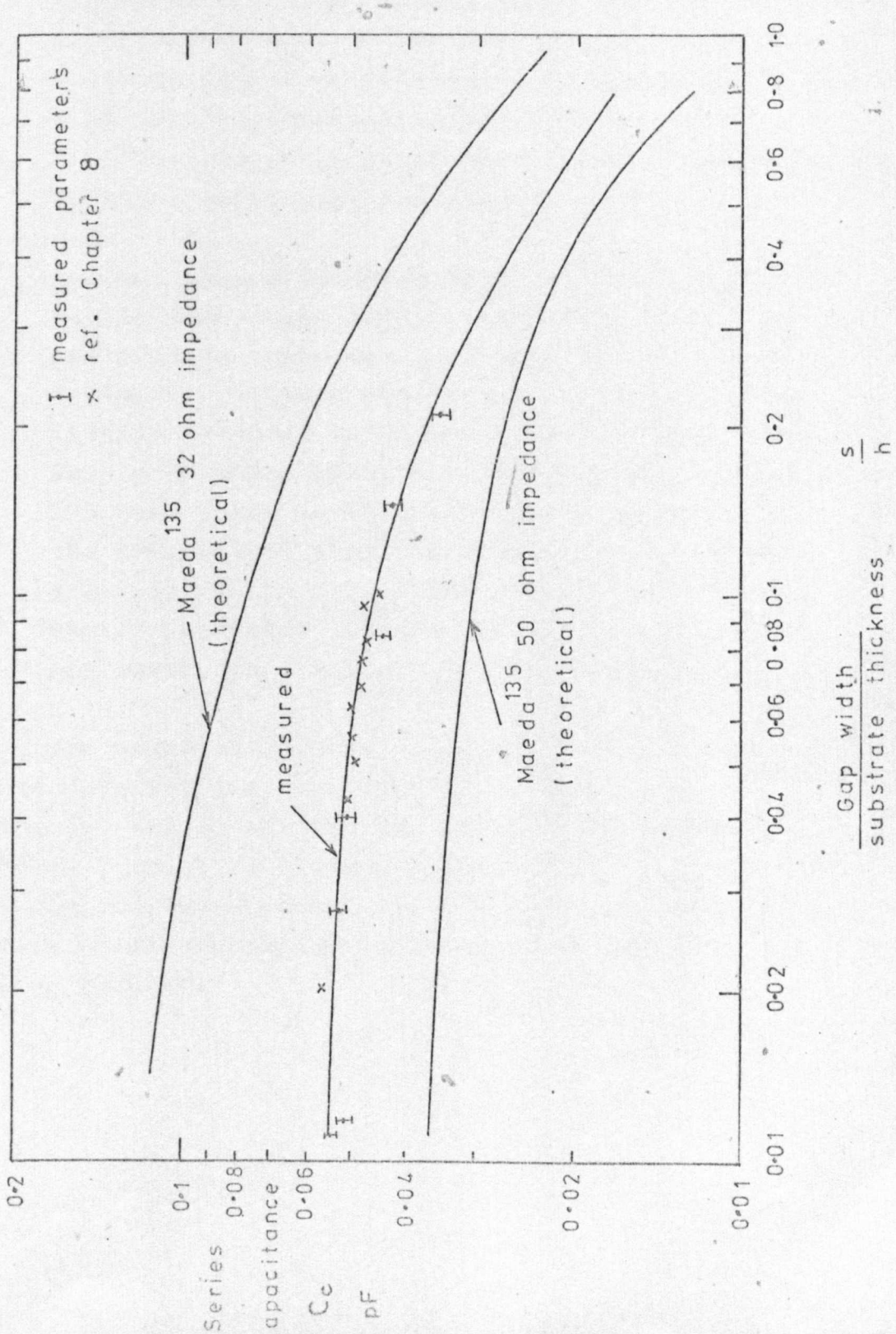
Sample	h (mm)	W_1 (mm)	W_2 (mm)	$\frac{W_1}{h}$	$\frac{W_2}{h}$	E_{eff1}	E_{eff2}	Z_1 (Ω)	Z_2 (Ω)	Resonant Frequency GHz	l (mm)	s (mm)	$\frac{s}{h}$	C_c pF
1	0·512	1·09	2·07	2·12	4·05	3·024	3·221	49·79	32·10	9·623157	12·49	0·006	0·0117	0·054
2	0·502	1·05	2·06	2·09	4·10	3·020	3·225	50·22	31·81	9·614992	12·53	0·009	0·018	0·0515
3	0·509	1·07	2·07	2·10	4·07	3·021	3·222	50·08	31·99	9·620275	12·51	0·014	0·0275	0·0527
4	0·498	1·06	2·05	2·13	4·11	3·025	3·226	49·65	31·75	9·588773	12·57	0·020	0·04	0·051
5	0·503	1·05	2·06	2·09	4·09	3·020	3·224	50·22	31·87	9·686780	12·52	0·043	0·085	0·044
6	0·510	1·08	2·08	2·11	4·08	3·022	3·223	49·94	31·93	9·675003	12·55	0·074	0·145	0·043
7	0·514	1·10	2·09	2·14	4·06	3·026	3·221	49·51	32·04	9·758633	12·53	0·108	0·210	0·035

FIGURE 4·23

Measured parameters of a gap-and-step discontinuity on quartz substrates at X band.

Gap series capacitance as a function of gap width to sustrate thickness ratio.

Microstrip line impedances : 50 and 32 ohms



4.5 Conclusions.

This chapter has investigated the properties of two types of microstrip discontinuities. These are

1) gap discontinuity (figure 4.1), in which a gap is introduced into a 32 ohm microstrip line. The gap width, s, is varied from approximately 5 μm to 100 μm. The equivalent circuit is given in figure 4.4, and graphs of the shunt capacitance, C_a, and the series capacitance, C_b, as functions of the ratio of gap width to substrate thickness, $\frac{s}{h}$, are given in figures 4.16 and 4.17 respectively.

   For the purposes of this project, the value of C_b is of particular importance.

2) gap-and-step discontinuity (figure 4.2), in which a gap is introduced into a microstrip line, which also includes an impedance step from 50 ohms to 32 ohms. A single frequency equivalent circuit of the discontinuity is shown in figure 4.18, but from the previously obtained results of the gap discontinuity, it has been shown to be sufficiently accurate to represent the discontinuity by the simple series capacitor, C_c, shown in figure 4.19. The value of this effective series capacitor is then plotted as a function of the gap width, in terms of $\frac{s}{h}$, in figure 4.23.

The measured results presented in this Chapter provide valuable data for the remainder of the work described in this thesis, and in particular, the results displayed in figures 4.17 and 4.23 provide important information for the design and operation of the measurement technique for thin film overlay capacitors, which is described in the following chapter.

5. DESIGN OF A MEASUREMENT TECHNIQUE FOR MICROWAVE OVERLAY CAPACITORS.

5.1 Introduction.

The major objective of the project described in this thesis is the fabrication and measurement of thin film overlay capacitors in the microwave frequency range. This chapter investigates possible techniques for the measurement of the characteristics of these components at 10 GHz; it discusses the advantages and disadvantages of methods currently in use, and outlines the design of a practical measurement system, developed by the author, which has an accuracy several times greater than the alternative techniques.

To permit the accurate design and operation of the measurements, extensive use has been made of the measured data of the transmission characteristics of microstrip and the characteristics of microstrip discontinuities, discussed in Chapters 3 and 4 respectively. Reference to these chapters, and to their corresponding data, will therefore be made where relevant.

5.2 Possible measurement techniques.

5.2.1. Impedance measurements.

The standard technique for precision impedance measurements is a slotted-line, and measurements have been made[142-144] up to 2.5 GHz, by connecting the test capacitor at the end of a microstrip line, and measuring the impedance on a GR-900 slotted-line (figure 5.1). Measurement of the reactance is relatively easy, although determination of the position of the minimum becomes increasingly difficult above 2.5 GHz. Evaluation of the Q factor requires the measurement of high V.S.W.R.'s, which in itself is difficult, and there are many losses to be accounted for, which introduce large corrections to the measured data, and limit the measurement accuracy.[145]

An extension of this slotted-line technique has

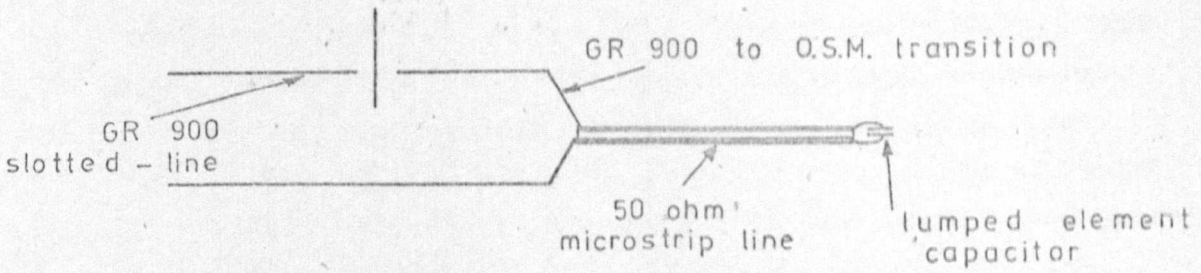


Figure 5·1 Slotted-line impedance measurement[142-144]

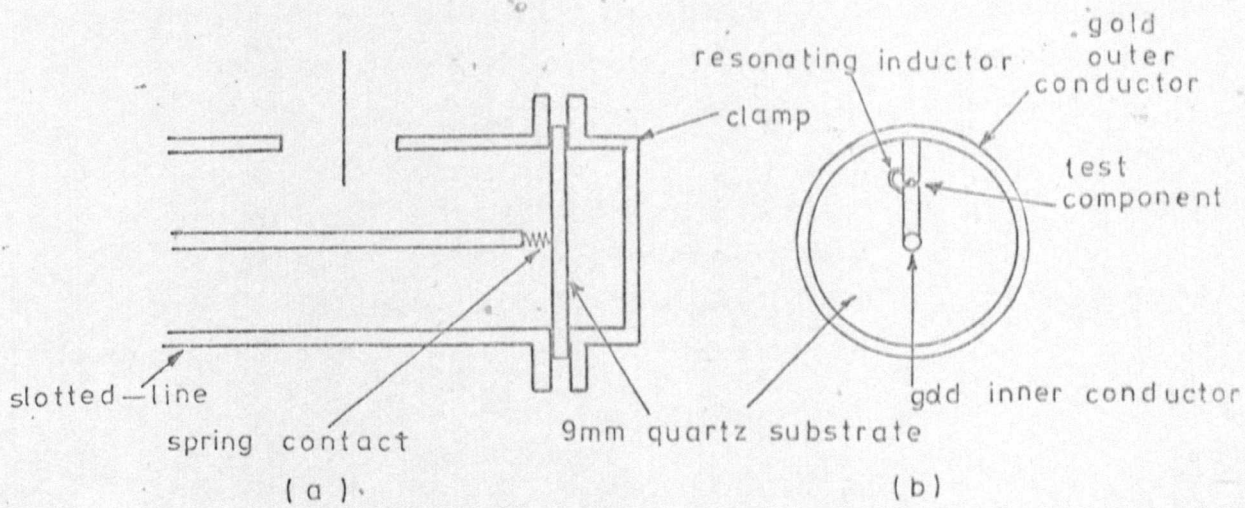


Figure 5·2 Slotted—line impedance measurement[146-147]

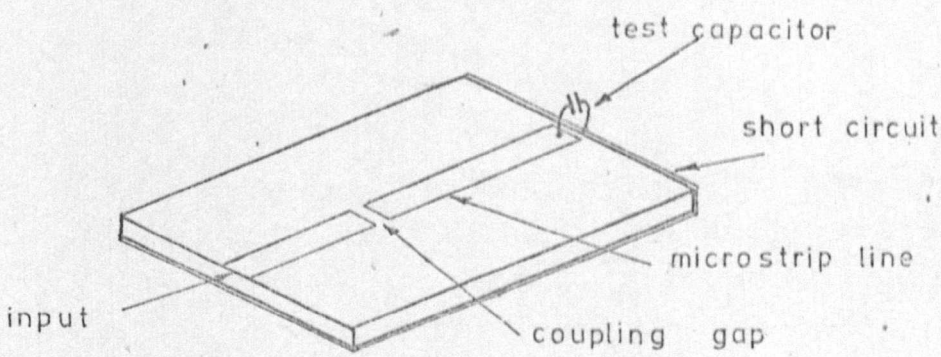


Figure 5·3 Microstrip resonator[98]

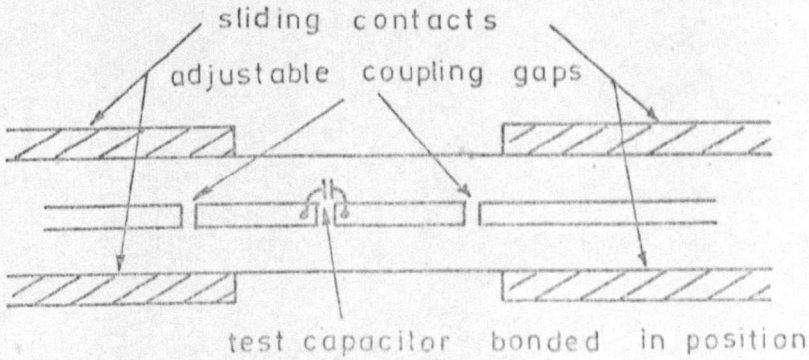


Figure 5·4 Coaxial resonator[145,150]

been adopted by several authors[3,146,147], where the test component is deposited on a 9 mm diameter quartz disc, which is connected at the end of a coaxial line (figure 5.2). The component is mounted between the inner and outer conductors (figure 5.2.b) and measurements using this technique have been made by these workers, up to 12 GHz. The value of test capacitance is obtained from the measured frequency, and the Q factor is derived from the measured resistance, and the rate of change of susceptance with angular frequency at resonance. Accuracy of measurement of capacitance is limited to approximately 9%, and Q measurements are unreliable due to the difficulty in measuring the large V.S.W.R's, and the relatively large loss of the inductor which is in shunt with the test capacitor[148].

Other impedance measurement techniques (e.g. bridges, network analyser etc.) are in general less accurate than slotted-line techniques, and therefore offer no advantages for this application.

5.2.2 Resonant techniques.

Resonant techniques[145] have been widely used for the measurement of material properties at microwave frequencies, as has already been indicated in Chapter 4. The resonator techniques rely on the test samples perturbing the Q and resonant frequency of a resonant cavity. Frequency shifts, determined fundamentally by the magnitude of the reactance of the test component, can be arranged to be large, and so measurement of the capacitance can be very accurate. Accuracy of measurement of the Q factor relies on the difference in Q factor before and after the test capacitor is inserted, and ideally, the resonant cavity should have a Q significantly larger than the test capacitor Q.

The major disadvantage of resonant techniques is that they are fundamentally single frequency measurements, although multiple resonances can be arranged to observe the frequency characteristics of the test components[149].

Caulton[98,145] describes a simple resonant technique in which the test element is connected at the end of a

microstrip resonant line. The line is capacitively coupled to the measurement system by a gap in the microstrip (figure 5.3). The resonant frequency and Q of the line with the element connected are measured, and measurements are repeated with the test component replaced by a short circuit. Measurements have been made by Caulton up to X band using this technique[145], but difficulty has been experienced in obtaining a good short circuit, and eliminating the effects of the component connecting leads.

An extension of this method, in which the capacitor is bonded in position in the centre of a microstrip line, is described by Hughes[149]. The losses of the microstrip lines are measured at the even modes of resonance, and the capacitor characteristics at the odd multiples of the fundamental frequency, but once again, the component characteristics are obscured by the bond-wire characteristics.

This technique has also been adapted for coaxial line [145,150] to take advantage of the higher unloaded Q factors available. In this method, the test component is connected across a gap in the centre conductor of an open-circuited half-wavelength resonator (figure 5.4). The resonator is used in the transmission mode, and the coupling is adjusted by sliding contacts which vary the size of the coupling gaps. The test capacitor is bonded in position, and the effects of the bond-wires are minimised by keeping the wires as short as possible.

The capacitor impedance, and the stray impedances, are calculated from a series of measurements. Firstly, the resonant frequency and Q of the resonant line in isolation are measured. Secondly, with the capacitor bonded in position, but short-circuited, the Q and inductance of the leads are found by measuring the Q and resonant frequency. Finally, with the capacitor connected across the gap, the Q and resonant frequency are again measured, and the value of capacitor Q and capacitance are then calculated.

The advantages of this particular technique are the high resonator Q factors available (approximately 1250 at 10 GHz), the low radiation losses, and the negligible dispersion. The disadvantages are, the doubtful effects

of the bond-wires, the components are not measured in a typical operational environment (due to the bond-wires), and the necessity for three measurements to determine the component properties.

Microstrip resonator.

Mehmet[19] has adapted Caulton's method to microstrip line, but the resonator is short-circuited at both ends (figure 5.5) to reduce radiation losses, and reflection rather than transmission techniques are used.

The test component can be connected to the resonant line in either one of two methods. The first method is by bonding, which introduces the undesirable bondwire effects encountered by Caulton. This method was not investigated by Mehmet; it is considered likely, however, that such a method would introduce significant errors due to the resistance and inductance of the bond-wires, and would also result in damage to the line, leading to complete line replacement after a small number of measurements. For these reasons, this method was not considered further.

The second method, and the method adopted by Mehmet, consists of simply placing the capacitor across the gap. The component is formed in such a way that a layer of dielectric is deposited on a metal-coated substrate, and positioned across the gap (figure 5.6.a) producing two "identical" capacitors in series (figure 5.6.b).

Mehmet's resonator has the advantage of simple design and construction, and due to the symmetrical nature of the resonant line, the test component properties can be easily determined. Also, by suitable choice of resonator dimensions, a series of measurements in X band can be made to observe any frequency effects of the component characteristics.

A disadvantage of the technique adopted by Mehmet is the major discontinuity introduced when the test component is inserted in the circuit, due to the necessarily large size of the capacitor support material. Further, the gap capacitance, C_g (figure 5.6.b), is altered by the addition of the capacitor chip, and is not therefore the same for both

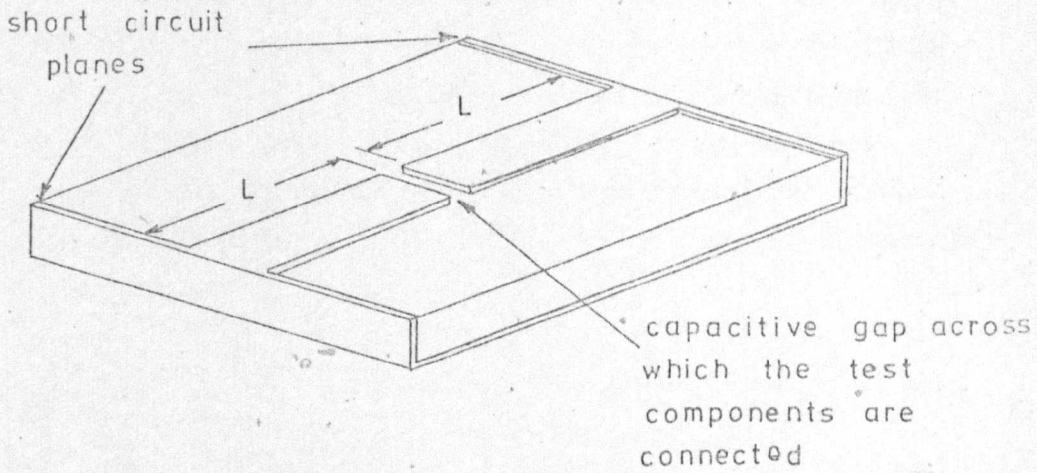


Figure 5·5 Mehmet's microstrip resonator[19]

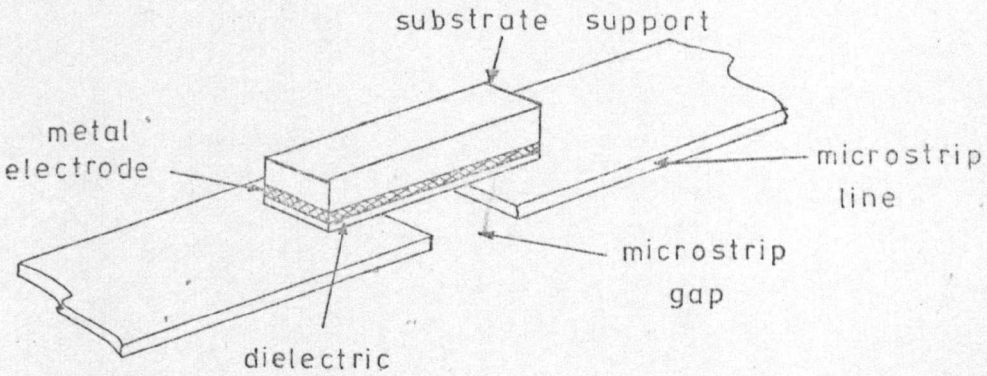


Figure 5·6 (a) Connection of test capacitor

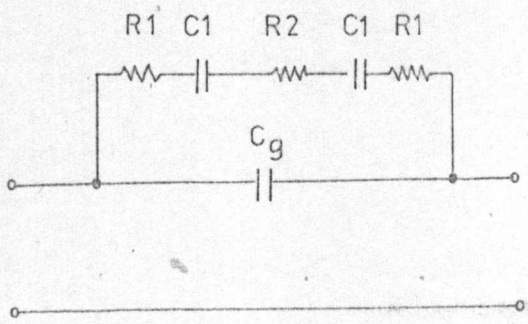


Figure 5·6 (b) Equivalent circuit of test capacitor and gap

measurements, leading to measurement errors. Mehmet also reported that pressure of contact between the test sample and the resonant line, and the effect of air gaps in series with the dielectric, produced variable measurement results, and coupled with the difficulty in accurately aligning the capacitor "chip" across the gap, repeatable results were impossible. These disadvantages therefore excluded this technique for the accurate measurement of the characteristics of overlay capacitors.

5.2.3 Summary.

The two techniques for the measurement of lumped elements which have generally been adopted by other workers in this field, are the coaxial resonator technique of Caulton[142], and the slotted-line technique of Aitcheson[146].

The resonator technique of Caulton's is simple and accurate, but the component characteristics are masked by the inductance and resistance of the bond-wires. Aitcheson's method, on the other hand, removes the bond-wire inaccuracies, but encounters the difficult task of measuring the resistance of high Q elements by slotted line-techniques, and also encounters contact resistance problems.

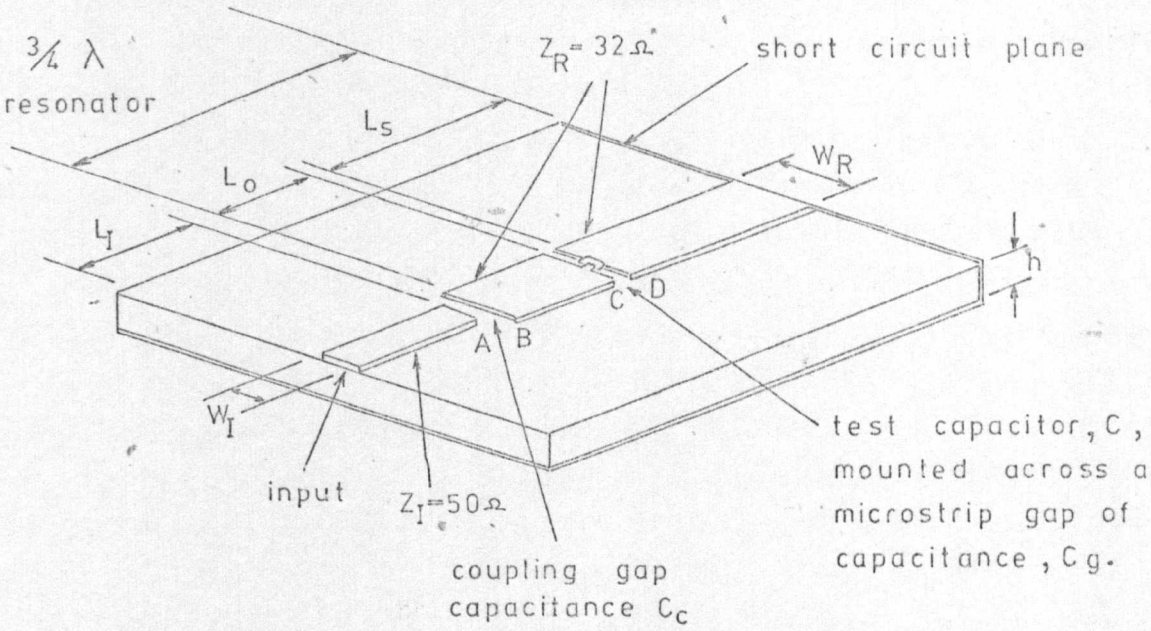
A desirable alternative technique, overcoming both of the major problems discussed above, would be one in which the characteristics of the component are measured by resonator techniques (as in Caulton's method), and in which no bond-wires are used for connecting the component to the resonator (as in Aitcheson's method).

In the following section, a technique will be described which includes both of these requirements, and also encompasses some of the advantages of previously mentioned techniques, and avoids many of the difficulties.

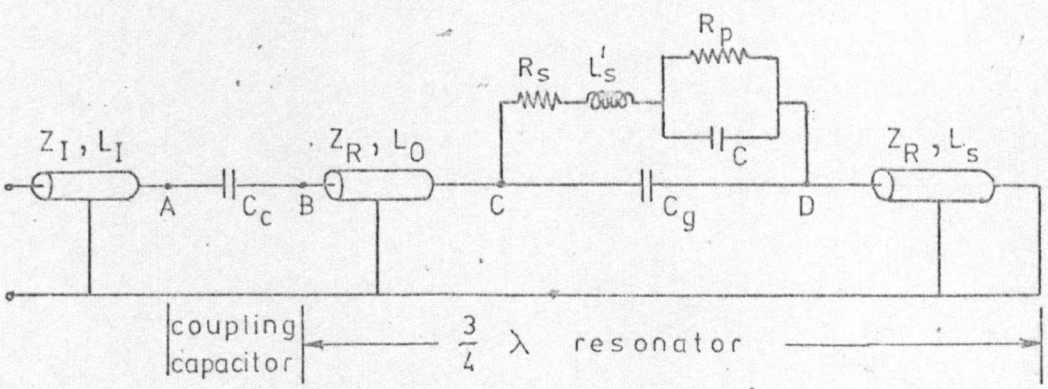
5.3 Proposed measurement technique.

The basic form of the measurement system adopted (figure 5.7) is a $\frac{3}{4}\lambda$ microstrip resonator, of 32 ohm characteristic impedance, into which the test capacitor is

Figure 5·7 Test resonator



(a) Schematic of microstrip resonator



where C is the test capacitance
R_p is the capacitor dielectric resistance
R_s is the capacitor electrode resistance
L_s' is the capacitor electrode inductance
C_c is the coupling gap capacitance
C_g is the capacitive gap capacitance
L_I, L_o, L_s, are the physical line lengths

(b) Equivalent circuit of the microstrip resonator

built as an inherent part of the resonant line. The resonator is short-circuited at one end, and at the other end, is coupled to a 50 ohm microstrip line by a gap in the transmission line. The complete circuit is fabricated on a 1" x 1" x 0.020" quartz substrate, and measurements of resonant frequency, return loss and Q factor, are made by connecting the 50 ohm microstrip line to a waveguide reflectometer, by the appropriate transitions.

As in the majority of resonator techniques, the resonator characteristics are determined without the test component inserted, and then the composite characteristics of the resonator plus the test capacitor are determined from a second measurement, with the test capacitor inserted. From the data obtained from both measurements, the test capacitor characteristics can be evaluated.

Reflection measurements were chosen in preference to transmission measurements, as it was anticipated that use would be made of the computer correction facilities of Shurmer[151], which at the time of development of the measurement technique, were available for reflection measurements only. With this computer correction facility, the overall measurement accuracy of the technique could be greatly improved as measurement system errors would be automatically taken into consideration.

The termination of the resonant line was selected as a short circuit in preference to an open circuit, as the losses due to radiation and resistance are considerably reduced[152-154].

As in Caulton's method[145], the coupling to the resonator can be adjusted (in this case by varying the width of the coupling gap) to obtain maximum measurement accuracy.

In the following sections, a detailed description is given of the resonator used in the measurement technique for overlay capacitors.

5.4 Detailed design of the measurement technique.

The design of the measurement technique can be divided into several discrete sections which can be studied substantially in isolation. These are;

1. the determination of the exact position for the test capacitor. This has a fundamental bearing on the adaptability and accuracy of the measurement technique.

2. the selection of the characteristic impedance of the resonant line, with a view to improving the measurement system accuracy.

3. the theoretical analysis of the equivalent circuit for the test capacitor.

4. the development of a theory for the microstrip gap when used as an admittance inverter.

5. the determination of the resonant conditions of the resonant line, with emphasis placed on the evaluation of the characteristics of the test capacitor.

6. the selection of the coupling gap width (and hence the measurement return loss) to optimise measurement accuracy.

7. the design of a shielding enclosure for the resonant line to reduce the radiation losses of the resonator.

Each of these features will be considered in detail in the following sections, and the resulting complete resonator will be discussed in section 5.4.8.

5.4.1 Test capacitor position.

The test capacitor can be positioned at any point along the resonant line. In Caulton's method[145], the test capacitor is positioned at the midpoint of the line, as this is the point of highest current density. Therefore insertion of the capacitor at this point has the greatest effect on the resonator Q and resonant frequency, and therefore maximum measurement sensitivity results.

In the $\frac{3}{4}\lambda$ resonator described here, the point of maximum sensitivity does not coincide with the centre of the microstrip line. Figure 5.8 shows voltage mode diagrams for the $\frac{3}{4}\lambda$ resonator, with various sizes of test capacitor inserted at the corresponding points of maximum measurement sensitivity. It can readily be seen that the capacitor position for maximum sensitivity is a function of the capacitance, and therefore, for a particular resonant line, a position can be found where the measurement system is most sensitive to a particular value of capacitance, and less sensitive to other values. This effect is demonstrated in figure 5.9, which shows the resonant frequencies of a resonator when test capacitors of varying magnitudes are located at varying distances (L_s) from the short-circuited end of the resonator. In figure 5.9.a, the overall resonator length is 13 mm, and in figure 5.9.b, the overall resonator length is 16 mm.

There are two distinct regions to each of these diagrams. Firstly, there is a region where a small change in the position of the capacitor has a large effect on the resonant frequency (i.e. $\frac{\partial f}{\partial l}$ is a maximum). This point also coincides with the most insensitive region for capacitance measurement (i.e. $\frac{\partial f}{\partial C}$ is a minimum). This generally is an unsatisfactory region to work in, as small errors in length measurement will have a large effect on the calculated value of capacitance.

The other region of the diagram is where $\frac{\partial f}{\partial C}$ is a maximum and $\frac{\partial f}{\partial l}$ is a minimum, and it is in this region that the capacitance measurements are most sensitive, and the measurements are most insensitive to errors in line length

Figure 5-8

EFFECT OF CAPACITOR SIZE ON THE POSITION OF MAXIMUM RATE OF CHANGE OF VOLTAGE

for a three-quarter wavelength resonator (C=∞)

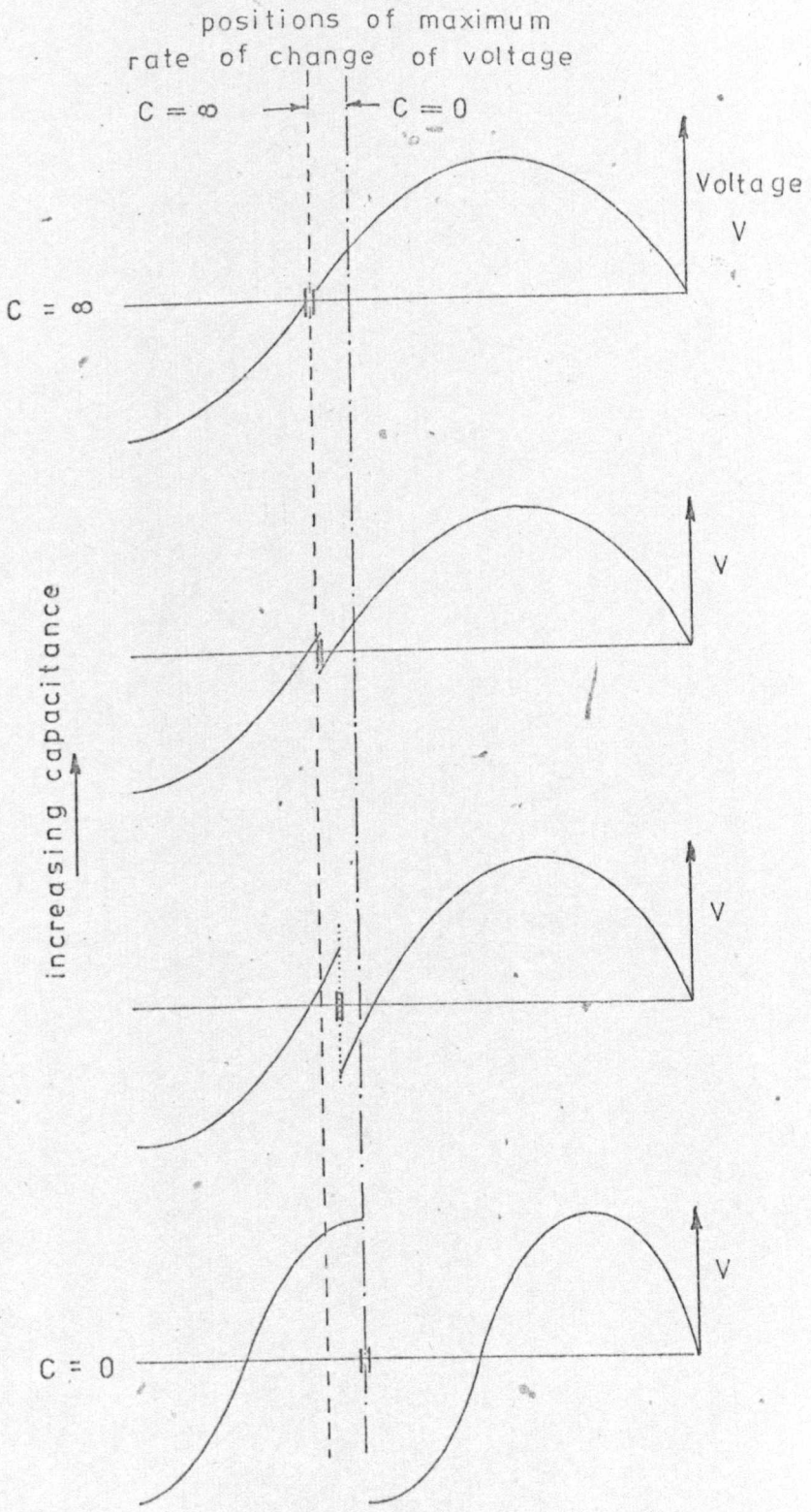
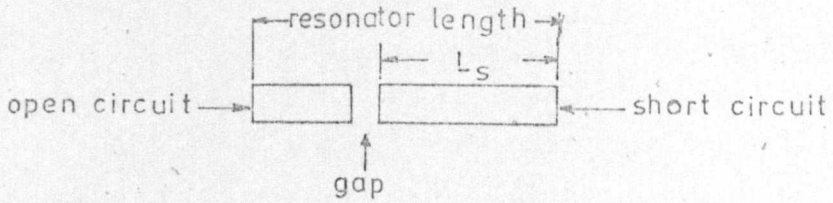


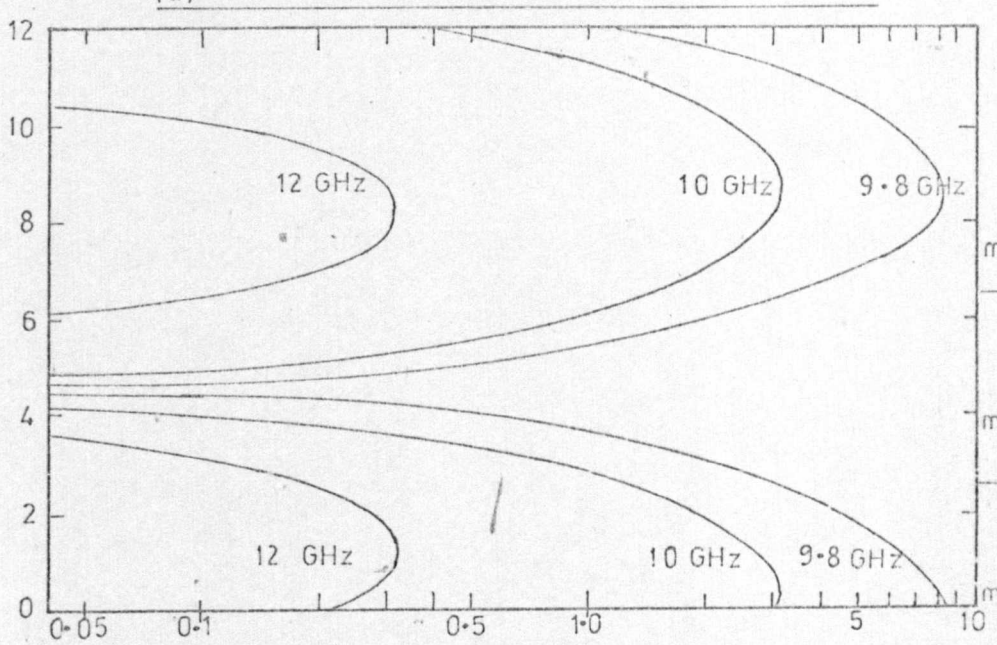
Figure 5·9

EFFECT OF CAPACITIVE-GAP POSITION ON THE RESONANT FREQUENCY OF A THREE-QUARTER WAVELENGTH RESONANT LINE

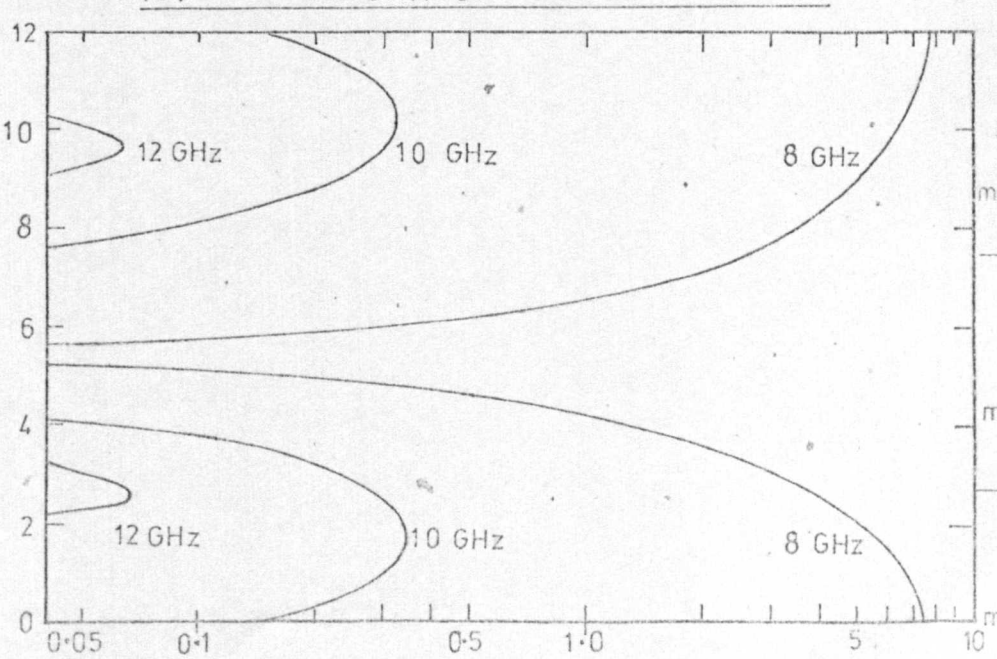


Substrate : Quartz Z_o : 32 ohms

(a) RESONATOR LENGTH 13 m.m.



(b) RESONATOR LENGTH 16 m.m.



DISTANCE OF GAP FROM SHORT CIRCUIT L_s (m.m.)

TOTAL SERIES CAPACITANCE AT THE GAP (pF)

measurement. The effect of the capacitor size on the position of maximum sensitivity is also shown in this diagram, by the peaks occurring at different values of L_s, for different values of capacitance.

The effect of a variation in the overall resonator length is, basically, to move the curves in the capacitance axis, as can be seen by comparison of figures 5.9.a and 5.9.b.

Determination of the resonator length.

The overall resonator length is chosen such that without the test capacitor inserted (i.e. with the gap capacitor, C_g, only in the circuit), the resonant frequency is within X band, and with the maximum size of test capacitor inserted in the circuit, the resonant frequency still remains within X band.

From measurements performed in Chapter 4 (figure 4.17) the capacitance of a gap in 32 ohm microstrip line has been shown to be approximately 0.08 pF, for a 25 μm gap.

A convenient value of test capacitance is approximately 1 pF, having taken into account the area required for the test capacitor, the processing facility capabilities, and the change in resonant frequency between the two measurements.

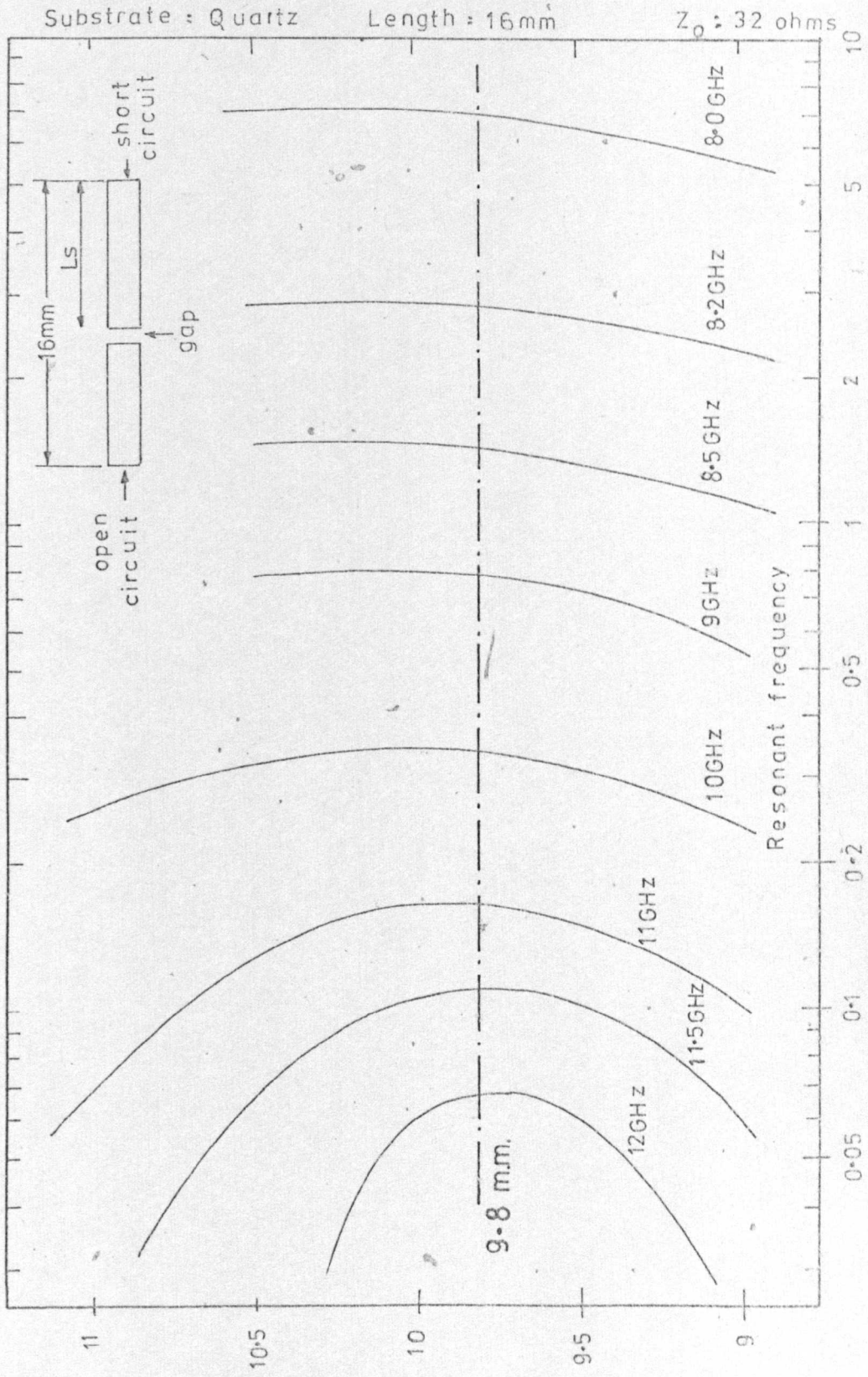
When the resonator is enclosed in a shielding box, a box resonance exists at approximately 8.25 GHz (Appendix 5.1), and hence the resonator length should be chosen to avoid measurements close to this frequency.

From the above requirements, and a study of various diagrams similar to those of figures 5.9.a and 5.9.b, but for resonators of varying lengths, it was decided that the most suitable resonator length would be 16 mm.

An enlarged diagram of figure 5.9.b for the 16mm resonator is given in figure 5.10. The most important requirement to satisfy at this stage of the design is that a suitable length, L_s, is selected such that both measurements (i.e. without, and with, the test capacitor in circuit) are performed in areas where $\frac{\partial f}{\partial C}$ is a maximum, and $\frac{\partial f}{\partial l}$ is a minimum (i.e. the flat portions of the curves of figure 5.10). From this diagram it can be seen that the optimum location

Figure 5·10

EFFECT OF CAPACITIVE-GAP POSITION ON THE RESONANT FREQUENCY OF A THREE-QUARTER WAVELENGTH RESONANT LINE



for the test capacitor is approximately 9.8 mm from the short-circuited end of the resonator. The resonant frequency, with a gap capacitor of 0.08 pF alone in the circuit, would be approximately 11.8 GHz, and with the 1 pF test capacitor inserted, would be approximately 8.6 GHz. Both resonant frequencies are therefore maintained within X band, but are sufficiently far removed from the anticipated box resonance at 8.25 GHz to avoid the difficulties associated with multiple resonances.

Having determined the optimum values of the resonator length and L_s, and using the anticipated value of gap capacitance, C_g, in the circuit of figure 5.7, the resonator equivalent circuit of figure 5.11 can be derived.

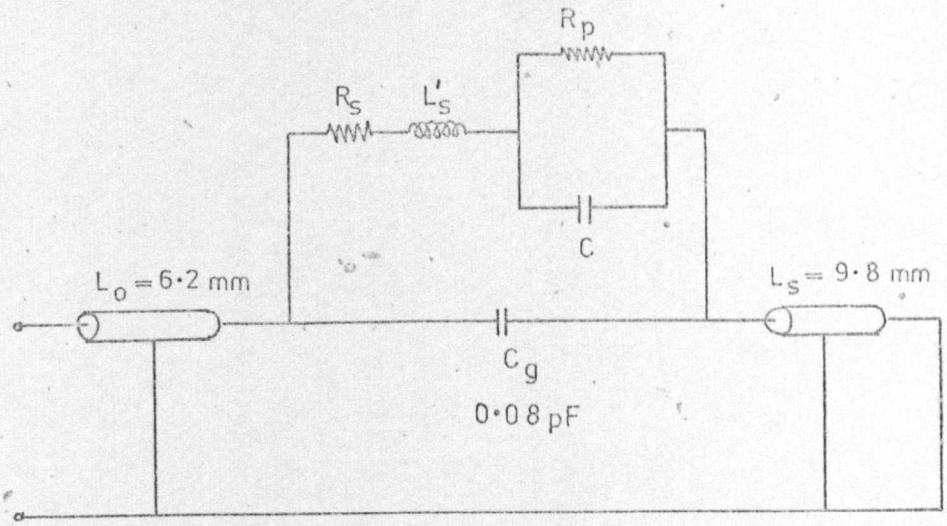
5.4.2 Resonator characteristic impedance.

The accuracy of the capacitor Q factor measurement is increased if the Q factor of the line is larger than that of the capacitor. With expected capacitor Q factors of several hundred[145], the Q of the unloaded microstrip line must, likewise, be at least several hundred.

However, a disadvantage indicated previously of the microstrip feeder system (Chapter 1), is the low Q factor obtainable when compared with other transmission media (e.g. waveguide, coaxial line), and to improve measurement accuracy, careful selection of the resonator impedance and conductor material must be made.

In Appendix 1.3, a relationship between the line impedance, the conductor conductivity and the resonator Q factor for microstrip lines was derived, and a graph showing this relationship was given in figure 1.8. From this figure it can be seen that the resonator Q factor is directly influenced by the conductor conductivity, and for this reason, bright copper electroplate, deposited from a copper sulphate bath, was used as the conductor material for the test resonators, as this was found to have the highest conductivity (46.7×10^6 mhos/metre) of various tested metal deposits[7].

A plot of the resonator Q factor, as a function of the impedance, for the particular resonator under consideration (without the test capacitor inserted) is shown in figure 5.12.



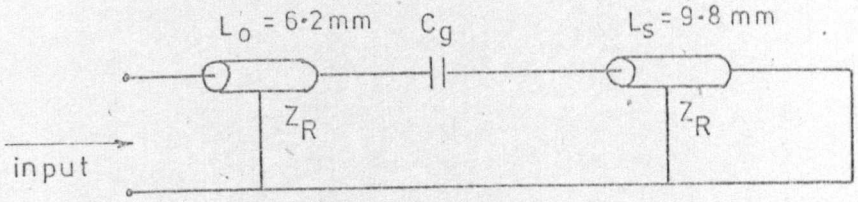
Resonant frequency without test capacitor $f_1 = 11{\cdot}8$ GHz

Resonant frequency with test capacitor $f_2 = 8{\cdot}6$ GHz

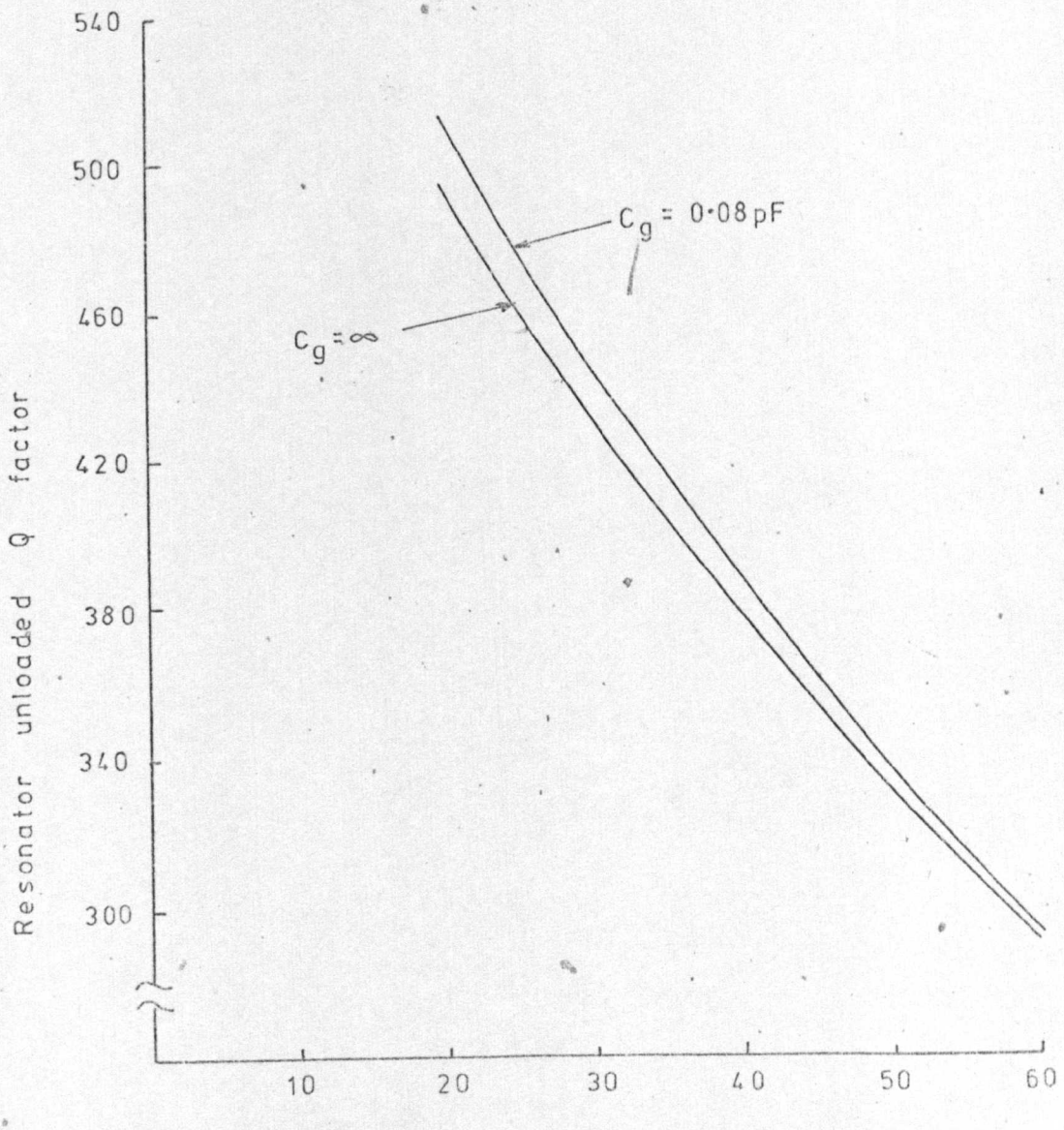
Figure 5·11 Resonator equivalent circuit

Figure 5·12

Microstrip resonator Q factor as a function of the characteristic impedance Z_R



substrate : quartz
dielectric constant : 3·78
substrate thickness : 0·5 mm
conductor conductivity : $46·7 \times 10^6$ mhos/metre
(bright copper plate)



The effect of the gap capacitance, C_g, is to increase the unloaded Q factor of the resonator by approximately 5%, due to the microstrip gap effectively decreasing the resonator length, and hence the losses, for a given resonant frequency.

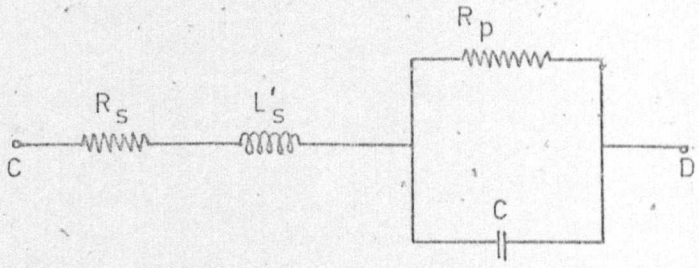
From figure 5.12 it can be seen that the Q factor increases with decrease in line impedance, but from figure 3.15 it will be recalled that the conductor width increases exponentially with decrease in Z. Zysman and Varon[110] have shown that in order not to decrease the value of effective dielectric constant when the resonator is enclosed in a shielding box, the ratio of shielding enclosure width to microstrip line width must be greater than 10, i.e. an impedance of greater than 27.5 ohms for a shielding enclosure for a 1" x 1" substrate. A compromise therefore exists between the Q factor and the impedance, and an impedance of 32 ohms, with a line width to substrate thickness ratio of approximately 4, was selected. The theoretical unloaded Q factor of the resonant line (figure 5.12) is therefore predicted to be approximately 435. However, from measurements on prototype resonator samples, the Q factors obtained for 32 ohm lines were in the region of 250, with the low values being attributed to processing factors.

In the ensuing design, therefore, calculations are based on expected Q factors of approximately 250, and not the theoretical value of 435.

5.4.3 Simplification of the equivalent circuit of the test capacitor and the microstrip gap.

The equivalent circuit adopted for the test capacitor in isolation is shown in figure 5.13. The equivalent circuit of the microstrip gap (section 4.3) across which the test capacitor is connected (figure 5.7) is shown in figure 5.14, and the complete circuit for the capacitor, and the gap, is shown in figure 5.15.

From measurements performed in section 4.3 on the characteristics of this particular microstrip gap, it has been shown (figures 4.16 and 4.17) that for a gap width of less than approximately 50 μm (i.e. $\frac{s}{h} \leq 0.1$), the value of shunt capacitance, C_a, is less than 6.5% of the series capac-



C = test capacitance

R_p = dielectric resistance

R_s = electrode resistance

L'_s = electrode inductance

Figure 5·13 Equivalent circuit of test capacitor

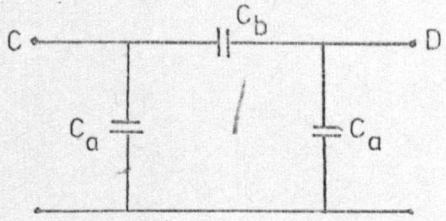


Figure 5·14 Equivalent ciruit of microstrip gap

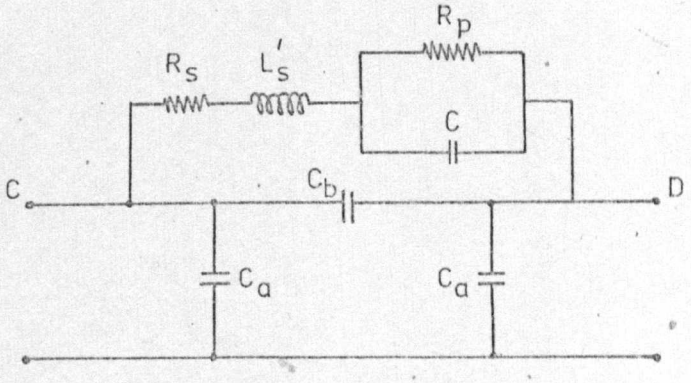


Figure 5·15 Equivalent circuit of test capacitor connected across the microstrip gap

itance, C_b. Under these circumstances, it has been shown (Appendix 5.2) that the exact equivalent circuit of figure 5.15 can be reduced to the simplified circuit of 5.16, where the microstrip gap π capacitor network has been replaced by an effective gap capacitance, C_g. The value of C_g of the simplified circuit is (Appendix 5.2), in this case, 6.5% larger than the value of C_b in the π equivalent circuit, but the resulting error in the measured value of test capacitance, C, due to the microstrip gap equivalent circuit simplification, is less than 0.16% for a 1 pF test capacitor, and a 50 μm gap.

Therefore, providing the gap width is maintained below 50 μm, there is negligible measurement error introduced if the effective gap capacitance, C_g, is used in preference to the rigorous equivalent circuit of figure 5.14, but there are, however, significant advantages to be gained due to the resulting simplification in the analysis of the resonator equivalent circuit.

The simplified equivalent circuit of figure 5.16 can then be reduced (Appendix 5.3) to the simple R-C circuit of figure 5.17, in which

$$R' = \frac{1 - \omega^2 CL'_s}{Q^* \omega C \left(1 + \frac{C_g (1 - \omega^2 CL'_s)}{C}\right)^2} \qquad 5.1$$

$$C' = \frac{C}{1 - \omega^2 CL'_s} + C_g \qquad 5.2$$

where Q^* is the capacitor Q factor.

From Appendix 5.3, it has been shown that

$$\frac{1}{Q^*} = \frac{1}{Q^*_E} + \frac{1}{Q^*_D} \qquad 5.3$$

where $$Q^*_E = \frac{1 - \omega^2 CL'_s}{\omega C R_s} \qquad 5.4$$

is the effective electrode Q factor, and

$$Q^*_D = \frac{Q_D^2 (1 - \omega^2 CL'_s)}{\omega C R_p} \qquad 5.5$$

is the effective dielectric Q factor, and

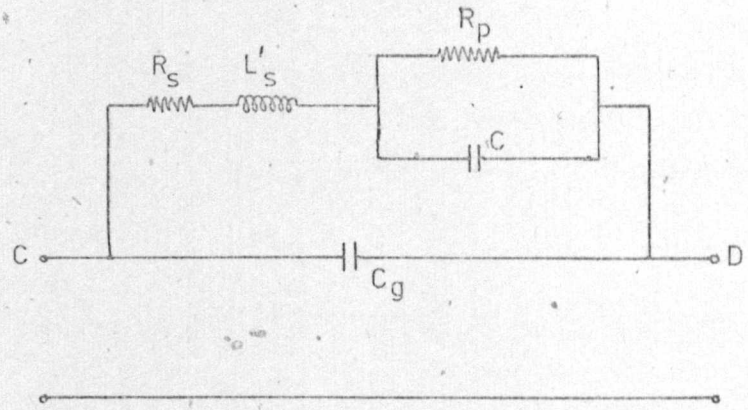


Figure 5·16 Reduced equivalent circuit of test capacitor and microstrip gap

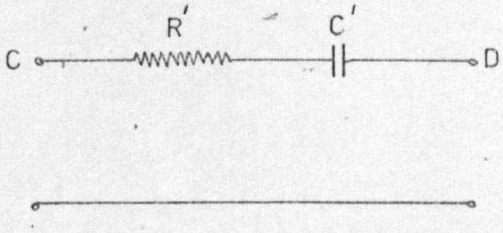


Figure 5·17 Reduced equivalent circuit of test capacitor and microstrip gap

$$Q_D = \omega C R_p \qquad 5.6$$

is the actual dielectric Q factor.

In all subsequent circuit analysis, therefore, equations 5.1 and 5.2 and the reduced equivalent circuit of figure 5.17 will be used to represent the test capacitor and the microstrip gap.

5.4.4 The microstrip gap as a coupling capacitor.

A series capacitor can be made to operate as an admittance inverter (i.e. it can transform a high impedance into a low impedance), and the absolute value of the transformed impedance is proportional to the series capacitance. In this particular application (figure 5.7), the coupling gap is used as an admittance inverter to transform the very high input impedance of the $\frac{3}{4}\lambda$ shunt resonant circuit (which is difficult to measure precisely), into a lower impedance, which can be measured to a much higher degree of accuracy. The width of the microstrip gap (i.e. the value of the series capacitance, C_c) is selected in such a way that the accuracy with which the transformed impedance can be measured, is optimised, taking into account the measurement technique and the measurement system errors.

This section outlines the theory and operation of the admittance inverter, and derives equations relating the coupling gap capacitance and the transformed impedance for the particular system under investigation.

Operation of the admittance inverter.

The series capacitor admittance inverter was initially reported by Matthaei[155], who quoted equations for the design parameters when the line impedances on both sides of the series capacitance are equal. In this application (figure 5.7.b), the impedances are not equal, and all design relationships for the admittance inverter have therefore had to be derived independently by the author.

An admittance inverter (figure 5.18) operates in such a way that a load admittance, Y_b, is seen at the input to the circuit as an admittance, Y_a, such that

$$Y_a = \frac{J^2}{Y_b} \qquad 5.7$$

where J^2 is a constant (with the dimensions of admittance) for a particular series capacitor at a particular frequency. Considering the shunt resonant circuit shown in figure 5.19, which is coupled to a measurement system with characteristic impedance, Z_I, by a coupling capacitor, C_c, then if the resonant circuit is referred to the input circuit, using equation 5.7, the circuit of figure 5.20 is obtained.

The unloaded Q factor of the resonant circuit of figure 5.19 is

$$Q_o = \omega C R \qquad 5.8$$

and the loaded Q factor of the resonant circuit of figure 5.20 is

$$Q_L = \frac{\frac{\omega C}{J^2}}{\frac{1}{J^2 R} + Z_I} = \frac{Q_o}{1 + J^2 R Z_I} \qquad 5.9$$

But by definition[156]

$$Q_L = \frac{Q_o}{1 + B} \qquad 5.10$$

where B is the coupling coefficient. Therefore, from equations 5.9 and 5.10

$$B = J^2 R Z_I \qquad 5.11$$

If $B < 1$ the circuit is undercoupled (figure 5.21.a)

$B = 1$ the circuit is critically coupled (figure 5.21.b)

$B > 1$ the circuit is overcoupled (figure 5.21.c)

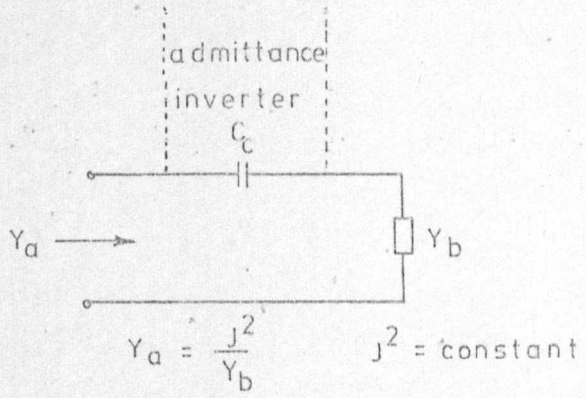


Figure 5·18 Admittance inverter

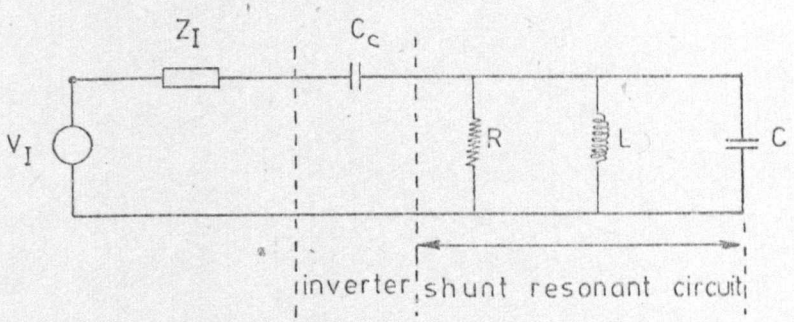


Figure 5·19 Shunt resonant circuit

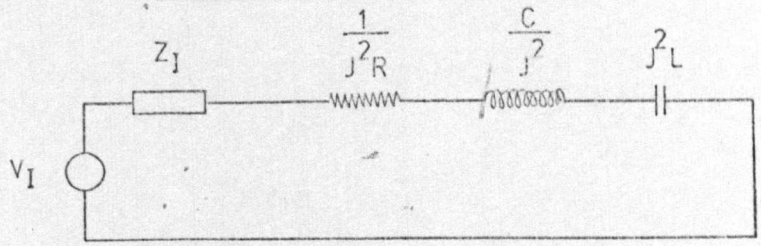
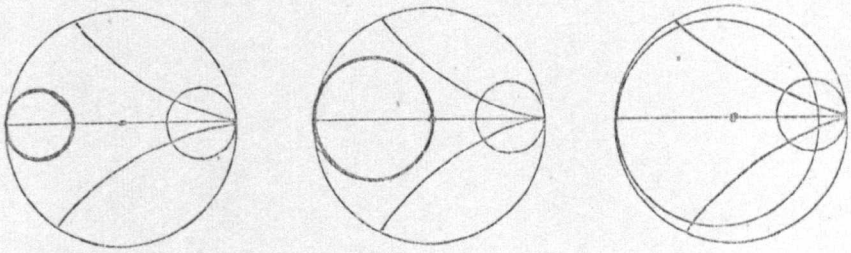


Figure 5·20 Inverted shunt resonant circuit



B < 1 undercoupled (a)

B = 1 critically coupled (b)

B > 1 overcoupled (c)

Figure 5·21 Smith chart admittance plots showing varying degrees of coupling

Therefore, by varying the size of the coupling capacitor, C_c, (i.e by varying J^2), the resonance curve of the circuit can be carefully controlled and varied, as desired, from undercoupled, through critically coupled, to overcoupled.

To enable the required value of coupling capacitor to be selected, the relationship between the coupling capacitor, C_c, and the constant, J^2, must be accurately determined, and this is effected in the following section.

Admittance inverter equations.

Matthaei[155] has shown that for a series capacitor to act as an admittance inverter, the exact equivalent circuit of the admittance inverter consists of a series capacitor, C_c, with two short lengths of transmission line on either side (figure 5.22). The expressions relating the gap capacitance, C_c, the line lengths, l_i and l_r, the impedances, Z_I and Z_R, and the coupling factor, J^2, are derived in Appendix 5.4, and are

$$\frac{1}{\omega C_c} = \frac{1}{J}\left[(1 - J^2 Z_I^2)(1 - J^2 Z_R^2)\right]^{\frac{1}{2}} \qquad 5.12$$

$$\tan|\beta_i l_i| = Z_I J\left[\frac{(1 - J^2 Z_R^2)}{(1 - J^2 Z_I^2)}\right]^{\frac{1}{2}} \qquad 5.13$$

$$\tan|\beta_r l_r| = Z_R J\left[\frac{(1 - J^2 Z_I^2)}{(1 - J^2 Z_R^2)}\right]^{\frac{1}{2}} \qquad 5.14$$

It will be observed that if $Z_I = Z_R$, then the equations reduce to those quoted by Matthaei.

For approximate practical design applications, these equations can be reduced to

$$\frac{1}{\omega C_c} = \frac{1}{J} \qquad 5.15$$

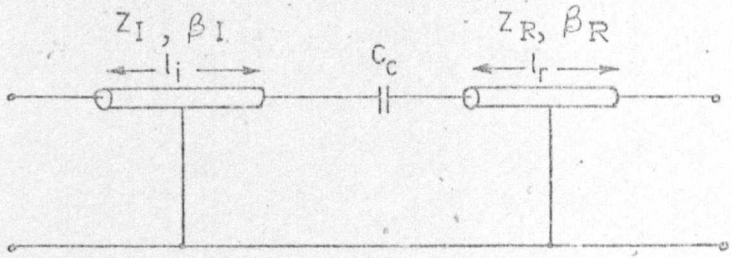


Figure 5·22 Admittance inverter equivalent circuit

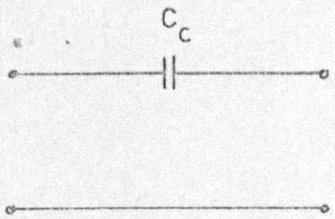


Figure 5·23 Coupling gap equivalent circuit

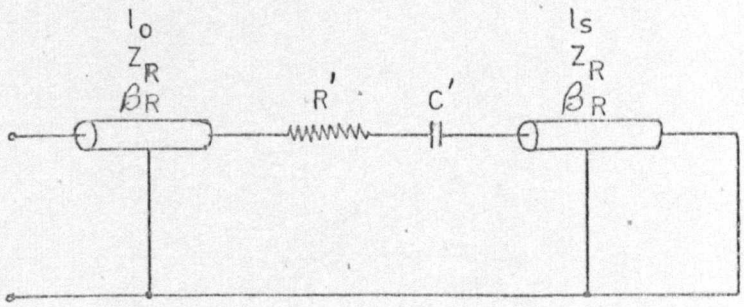


Figure 5·24 Reduced equivalent circuit of resonator

$$l_i = - Z_I v_i C_c \qquad 5.16$$

$$l_r = - Z_R v_r C_c \qquad 5.17$$

where v_i and v_r are, respectively, the velocities of propagation in the primary line of impedance Z_I, and in the secondary line of impedance, Z_R.

As is shown in equations 5.16 and 5.17, the line lengths, l_i and l_r, are small and negative, and must be absorbed into the circuits on either side of the series capacitor.

In the following section, the operation of a microstrip gap as as admittance inverter will be described.

The microstrip gap as an admittance inverter.

It has been shown (Appendix 4.6) that the exact equivalent circuit of a microstrip gap (figure 4.2) can be approximated by a simple equivalent series capacitor (figure 5.23).

In section 4.4, the characteristics of this equivalent series capacitor for the particular microstrip gap used in this application were investigated, and a plot of series capacitance, C_c, as a function of the corresponding microstrip gap width (in terms of $\frac{s}{h}$) was given in figure 4.23.

In the particular application under consideration, the optimum value of J^2 will be determined at a later stage, (section 5.4.6), and then, using equations 5.12 - 5.14, the required values of l_i, l_r, and C_c for the coupling capacitor can be determined. Then the coupling capacitor, C_c, can be related to the physical microstrip circuit, using the data of figure 4.23.

To verify the basic theory of the coupling capacitor, and to test the operation of the microstrip gap as an admittance inverter, two simple tests were carried out.

In the first of these, a short length of short-circuited coaxial line was connected to a coaxial reflect-

ometer, and the line was capacitively coupled to the system by slightly unscrewing the APC-7 connector. The resonance curve was displayed on a polar display. The coupling capacitance was slowly increased by lightly tightening the connector, and the resonance curve could be seen to vary from undercoupled, through critically coupled, to overcoupled. The frequency effects of the negative line lengths (equations 5.16 and 5.17) were also observed by a small decrease in the resonant frequency as the coupling capacitor was increased.

The second test involved a microstrip resonator, coupled to a 50 ohm input line by a microstrip gap. The resonant frequency and coupling coefficient were measured initially, and then a small piece of alumina (0.655x2x5mm) was placed edge-on across the gap, thereby increasing the gap capacitance. With the alumina in position, the degree of coupling was seen to increase and the resonant frequency decrease, further substantiating the correctness, in general form, of the equations 5.12 - 5.17.

In order to determine the value of J^2 required for the capacitor measurements, the conditions at resonance for the two measurements (i.e. with and without the test capacitor inserted) must be derived, and this is undertaken in the following section.

5.4.5 Derivation of resonance conditions.

The equivalent circuit of the $\frac{3}{4}\lambda$ resonator shown in figure 5.7 is given in figure 5.24, where the test capacitor and the microstrip gap across which it is connected, have been represented by the series equivalent circuit derived in section 5.4.3.

At the resonant frequency $\omega=\omega_o$, it has been shown (Appendix 5.5) that

$$\frac{1}{\omega_o C' Z_R} = \tan\beta l_s - \cot\beta l_o \qquad 5.18$$

The coupling coefficient, B, at resonance is (Appendix 5.5)

$$B = \frac{J^2 Z_I Z_R \operatorname{cosec}^2 \beta l_o}{\frac{R'}{Z_R} + \alpha_o m_o} \qquad 5.19$$

where α_o = the attenuation constant

$$m_o = l_o \operatorname{cosec}^2 \beta l_o + l_s \sec^2 \beta l_s \qquad 5.20$$

and the unloaded Q factor, Q_o, is given by (Appendix 5.5)

$$Q_o = \frac{\frac{\omega_o}{2}\left[\frac{m_o}{v} + \frac{1}{\omega_o^2 C' Z_R}\right]}{\frac{R'}{Z_R} + \alpha_o m_o} \qquad 5.21$$

Variation of resonator parameters with frequency.

It will be recalled from section 5.4.1 that for the initial measurement, without the test capacitor in the circuit, the resonant frequency is approximately 11.8 GHz, and for the second measurement, with the test capacitor inserted, the resonant frequency is approximately 8.6 GHz. If the characteristics of the test capacitor are to be accurately evaluated, the effects of the frequency change on the characteristics of the resonator must be determined and taken into account in the measurements. With this intention, the following assumptions have been made;

1. the gap capacitors, C_c and C_g, do not vary with frequency.

2. the value of J^2 varies with frequency as described by equation 5.12.

3. the effective dielectric constants of the microstrip lines vary linearly with frequency, within the frequency range of interest. This has been substantiated in section 3.5.1.

4. the microstrip line impedances, as derived using Schneider's equations (equations 3.1 - 3.2) do not vary with frequency, but the actual characteristic impedances, as described by equation 3.3, do vary with frequency, due to the frequency dependence of E_{eff} as described above.

5. the attenuation constant, α, is frequency dependent, and it has been shown (Appendix 5.6) that

$$\frac{\alpha_1}{\alpha_2} = \left(\frac{\omega_1 \, E_{eff1}}{\omega_2 \, E_{eff2}} \right)^{\frac{1}{2}} \qquad 5.22$$

where suffix 1 denotes parameters at frequency ω_1
and suffix 2 denotes parameters at frequency ω_2

6. it will be recalled from section 5.4.4, that the negative line lengths, l_i and l_r, associated with the admittance inverter, are frequency dependent. This, therefore, introduces frequency dependence on the line length, l_o, (figure 5.24), since

$$l_o = L_o + l_r \qquad 5.23$$

where L_o is the physical length of microstrip line (figure 5.7)

l_r is the length of line associated with the admittance inverter (figure 5.22)

l_o is the effective length of line for the resonator (figure 5.24).

Therefore, for the initial measurement at the

frequency, ω_1, at which $C'=C_g$ and $R'=0$, and suffix 1 denotes parameters at the frequency, ω_1, we have, from equations 5.18 - 5.22

$$\frac{1}{\omega_1 C_g Z_{R1}} = \tan\beta_1 l_s - \cot\beta_1 l_{o1} \qquad 5.24$$

$$B_1 = \frac{J_1^2 Z_{I1} Z_{R1} \mathrm{cosec}^2 \beta_1 l_{o1}}{\alpha_1 m_1} \qquad 5.25$$

$$Q_1 = \frac{\frac{\omega_1}{2}\left[\frac{m_1}{v_1} + \frac{1}{\omega_1^2 C_g Z_{R1}}\right]}{\alpha_1 m_1} \qquad 5.26$$

where $$m_1 = l_{o1}\mathrm{cosec}^2 \beta_1 l_{o1} + l_s \sec^2 \beta_1 l_s \qquad 5.27$$

For the second measurement, at frequency ω_2, with the test capacitor inserted, R' and C' are given by equations 5.1 and 5.2, suffix 2 denotes parameters at the frequency ω_2, and the resonant conditions are;

$$\frac{1}{\omega_2 C'_2 Z_{R2}} = \tan\beta_2 l_s - \cot\beta_2 l_{o2} \qquad 5.28$$

$$B_2 = \frac{J_2^2 Z_{I2} Z_{R2} \mathrm{cosec}^2 \beta_2 l_{o2}}{\frac{R'_2}{Z_{R2}} + \alpha_2 m_2} \qquad 5.29$$

$$Q_2 = \frac{\frac{\omega_2}{2}\left[\frac{m_2}{v_2} + \frac{1}{\omega_2^2 C'_2 Z_{R2}}\right]}{\frac{R'_2}{Z_{R2}} + \alpha_2 m_2} \qquad 5.30$$

where $$m_2 = l_{o2}\mathrm{cosec}^2 \beta_2 l_{o2} + l_s \sec^2 \beta_2 l_s \qquad 5.31$$

Failure to take into account the frequency effects outlined above will lead to errors of up to 1% in capacitance measurement, and 33% in Q factor measurement.

5.4.6 Selection of the degree of coupling.

In the previous section, relationships were derived between the coupling coefficient, B, and the admittance inverter parameter, J^2. In this section, a suitable value of B, and hence the coupling capacitor, C_c, will be selected for use in the measurement of thin film overlay capacitor properties.

The return loss at resonance is related to the coupling coefficient by the expression

$$\text{return loss} = -10\log_{10}\left(\frac{1 - B}{1 + B}\right)^2 \qquad 5.$$

and for the particular resonator under consideration (figure 5.7), without the test capacitor in the circuit, the return loss at resonance is given by (equations 5.25, 5.26 and 5.32)

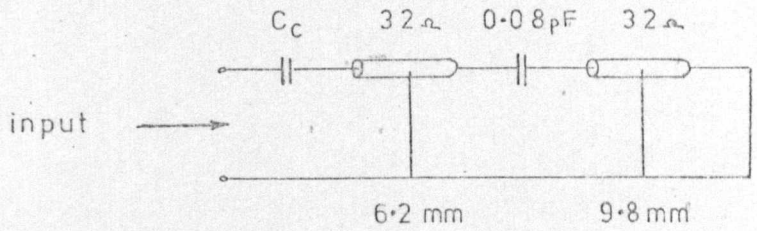
$$\text{return loss} = -20\log_{10}\frac{1 - \dfrac{2J_1^2 Z_{I1} Z_{R1} Q_1 \operatorname{cosec}^2 \beta_1 l_{oi}}{\beta_1 m_1 + \dfrac{1}{\omega_1 C_g Z_{R1}}}}{1 + \dfrac{2J_1^2 Z_{I1} Z_{R1} Q_1 \operatorname{cosec}^2 \beta_1 l_{oi}}{\beta_1 m_1 + \dfrac{1}{\omega_1 C_g Z_{R1}}}} \qquad 5.33$$

Then, using equation 5.33, and the equation relating the admittance parameter, J^2, and the coupling capacitor, (equation 5.12), a plot of return loss at resonance, as a function of the resonator Q factor, for various values of coupling capacitor, can be made, and is given in figure 5.

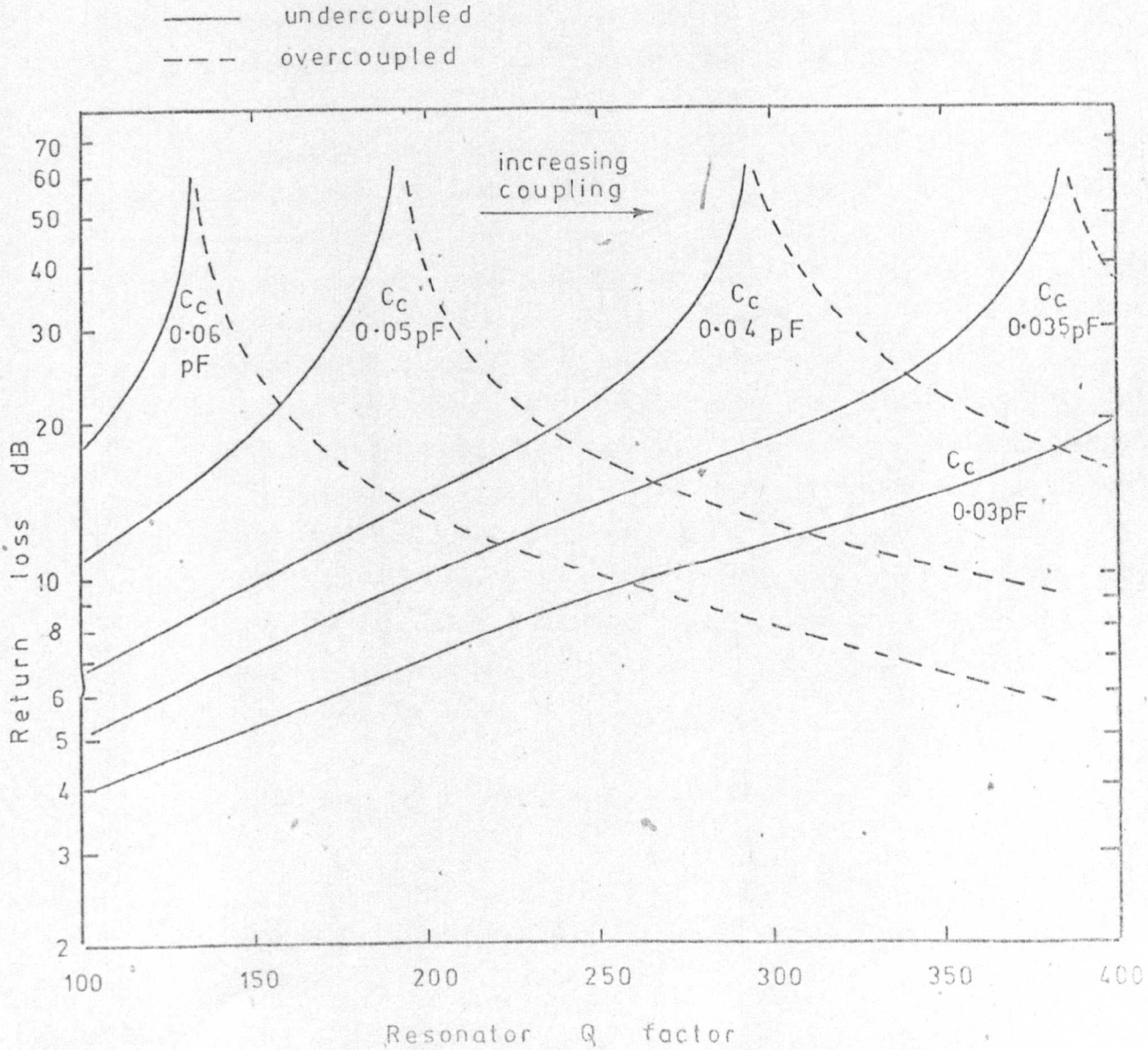
Similarly, with a test capacitor, C, inserted in the circuit, it can be shown that the return loss at resonance

Figure 5·25

Theoretical return loss of a resonator as a function of the resonator unloaded Q factor for selected values of coupling capacitance, C_c. (equation 5·33)



resonant frequency = 11·8 GHz



given by (equations 5.29, 5.30 and 5.32)

$$\text{return loss} = -20\log_{10} \frac{1 - \dfrac{2J_2^2 Z_{I2} Z_{R2} Q_2 \operatorname{cosec}^2 \beta_2 l_{o2}}{\beta_2 m_2 + \dfrac{1}{\omega_2 (C + C_g) Z_{R2}}}}{1 + \dfrac{2J_2^2 Z_{I2} Z_{R2} Q_2 \operatorname{cosec}^2 \beta_2 l_{o2}}{\beta_2 m_2 + \dfrac{1}{\omega_2 (C + C_g) Z_{R2}}}} \qquad 5.34$$

A plot of the return loss at resonance as a function of the composite Q factor of the microstrip and the test capacitor is then shown in figure 5.26.

As indicated previously, practical Q factors of prototype resonators, without the test capacitor inserted, are of the order of 250, and with a 1pF test capacitor (with a capacitor Q of 100) inserted in the circuit, the composite Q factor can be calculated (equation 5.30) to be approximately 150.

To minimise errors in Q factor measurement due to noise, drift and the variation in the base-line of the resonance curve (Chapter 8), it was considered preferable to maintain the return loss at resonance, for both measurements, above approximately 10 dB. Then, taking into consideration this return loss limit, the predicted Q factors for both measurements, and the limitation previously imposed (Chapter 4) that the ratio of coupling gap width to substrate thickness should not be greater than 0.1 (i.e. $C_c > 0.045$pF), a suitable value for the coupling capacitor for this application, is 0.045pF, which requires a gap width of 50 μm (figure 4.23).

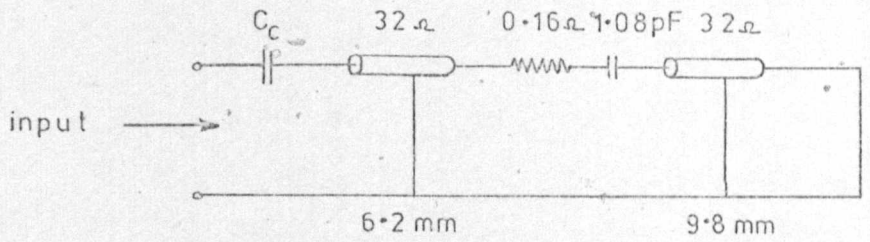
This value of capacitance maintains both circuits undercoupled, with a minimum return loss (for the second measurement) of 12 dB.

5.4.7 Design of a shielding enclosure.

To minimise radiation from the resonator, the resonant line was enclosed in a brass shielding enclosure. The

Figure 5·26

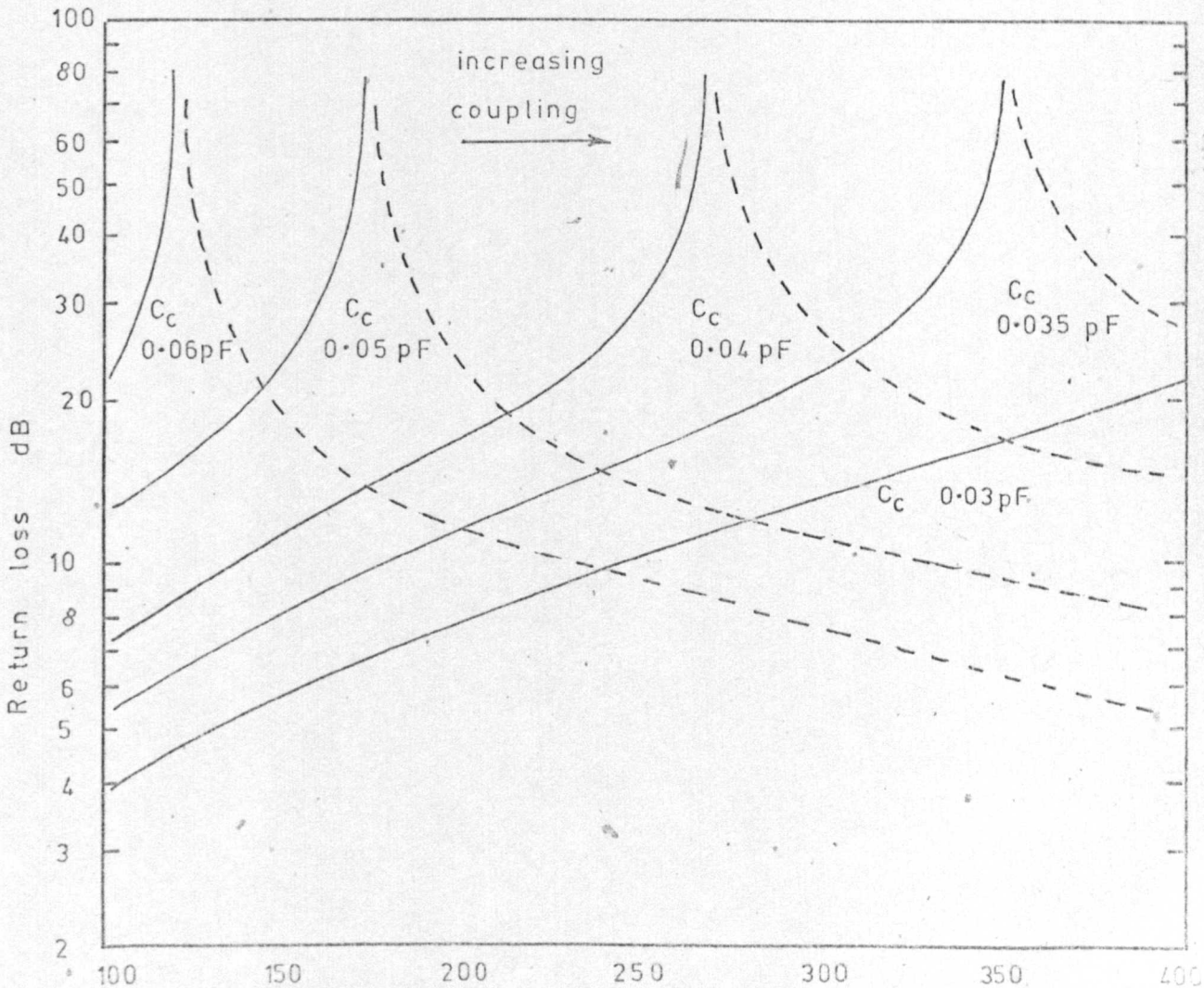
Theoretical return loss of a resonator as a function of the resonator unloaded Q factor for selected values of coupling capacitance, C_c (equation 5·34)



test capacitance = 1·0 pF ; Q factor = 100 ;
resonant frequency = 8·6 GHz

—— undercoupled

– – – overcoupled



main features in the design of the enclosure are;

1. electrical connection to the microstrip line is made without soldering or bonding, so that the connectors can be removed and replaced without damage being caused to the line.

2. connection between the waveguide reflectometer and the microstrip line is made with the minimum number of transitions, so that unwanted reflections can be minimised.

   The most suitable commercially available transitions were waveguide to APC-7 adapters (model HP X281B) and the APC-7 to microstrip connector (model O.S.M. 14493A), which were selected because of their rigidity and their electrical characteristics.

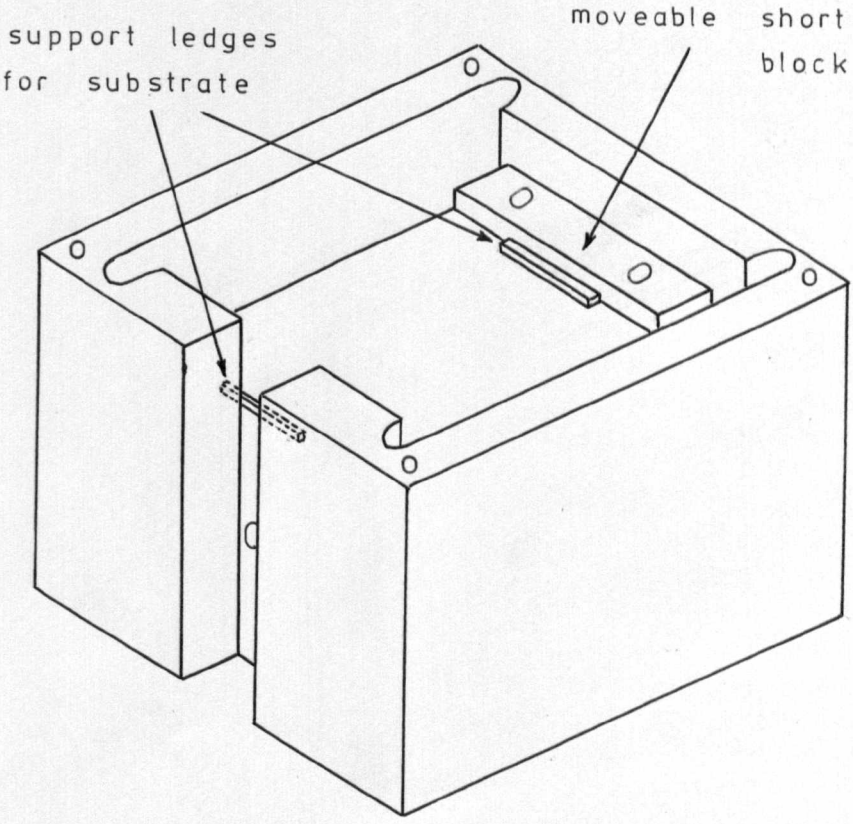
A detailed diagram of the shielding enclosure is given in figure 5.27.a, and a photograph of the box, with a test substrate inserted, is shown in figure 5.27.b.

To ensure a good reproducible electrical contact between the microstrip ground plane and the enclosure, the substrate is supported at only two points, i.e. two ledges 0.5mm long and 5mm wide, at the front and back edges of the substrate (figure 5.27.a). It was found to be of great importance to machine these ledges to a high degree of accuracy, as a variation of up to 25 μm in taper across the 1 inch square substrate was sufficient to produce lack of reproducibility of the Q factor measurements.

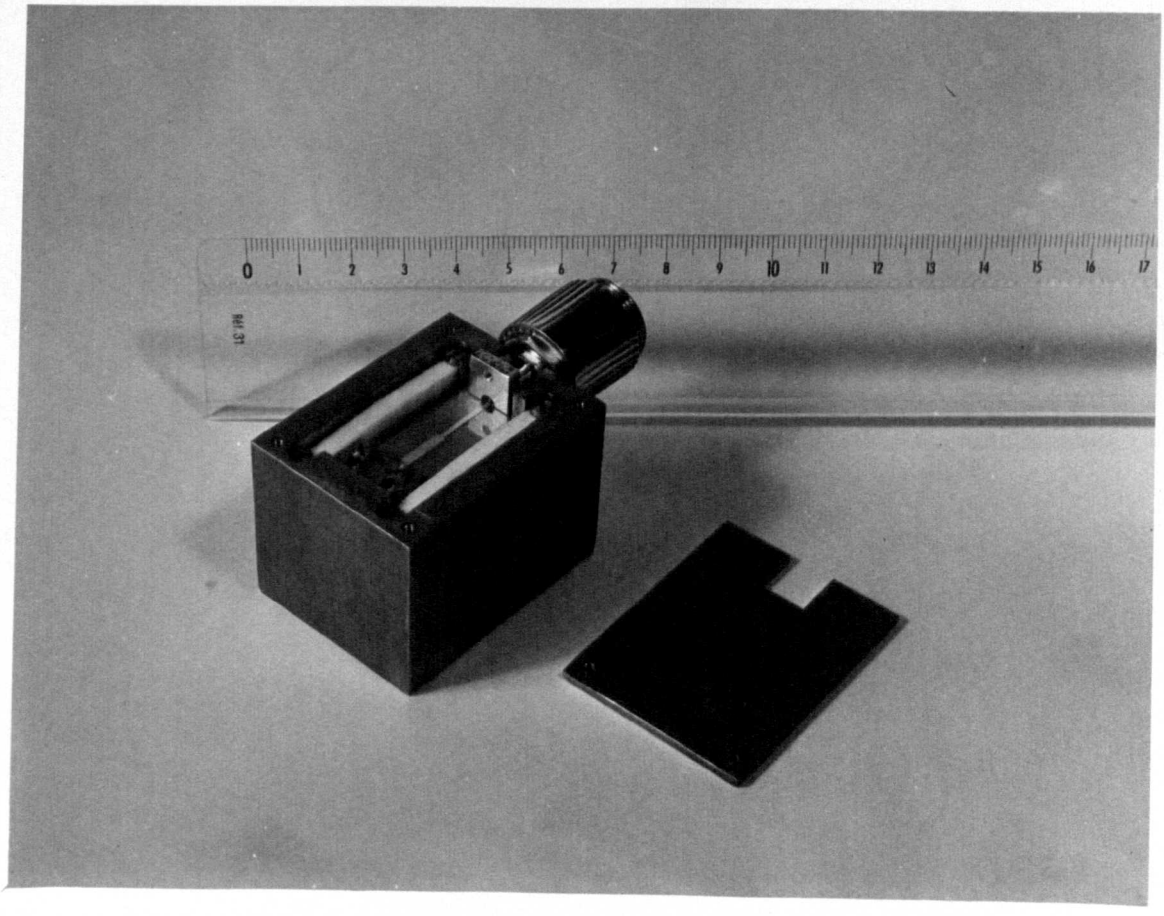
To prevent substrate movement, the substrate is held in position by two P.T.F.E. strips along the sides of the box, which are secured by screws.

To ensure that the fringing fields at the end of the microstrip line are effectively short-circuited, a brass block, which can be adjusted in position, is provided at the short-circuited end of the microstrip line.

It has been shown (section 5.4.2) that to ensure the enclosure does not affect the effective dielectric constant of the microstrip lines, then, in figure 5.28



(a)



(b)

Figure 5·27 Shielding enclosure for the test resonator

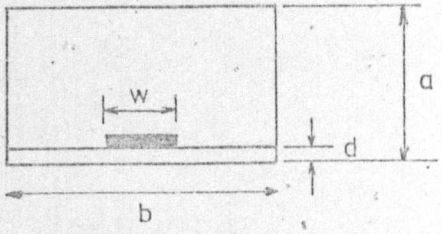
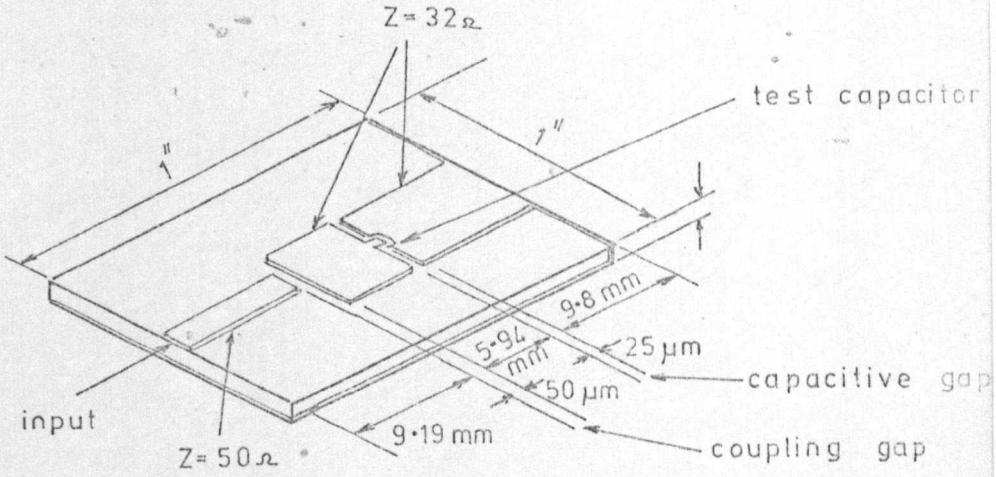
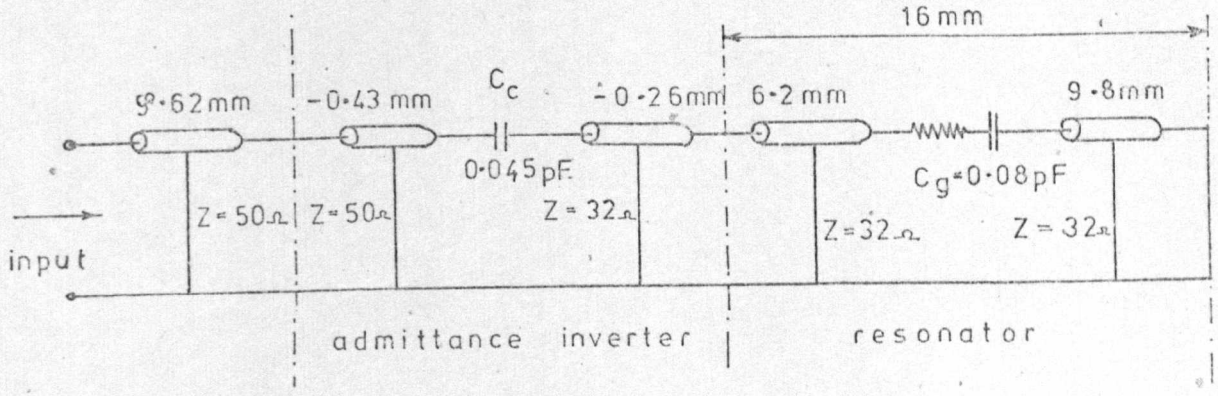


Figure 5·28 Critical dimensions of the shielding enclosure



(a) Schematic of the complete resonator



(b) Equivalent circuit of the complete resonator

Figure 5·29 The complete test resonator

$\frac{b}{w}$ must be greater than 10

Further, Kowalski[117] has shown that

$\frac{a}{d}$ must be greater than 5

and $\frac{b}{d}$ must be greater than 10.

For the particular shielding enclosure described here

$\frac{b}{w} = 12.75$; $\frac{a}{d} = 11$; $\frac{b}{d} = 51$;

and therefore the shielding enclosure will have negligible effect on the effective dielectric constant of the resonant lines.

The APC-7 to microstrip transition is mounted as a sliding fit in a slot to permit ease of assembly. The transition is secured in position by a single screw.

As indicated above, the shielding enclosure has a resonant frequency at 8.25 GHz (Appendix 5.1) which is the only box resonance occurring in X band.

5.4.8 The completed test resonator.

In the preceding sections, a detailed design of the various elements of the resonator has been given, and the resulting complete resonator is shown in figure 5.29.

The main features of the complete resonator are then;

1. the resonator is fabricated on a 1"x 1"x 0.020" quartz substrate.

2. the input line impedance is 50 ohms, and the resonator line impedance is 32 ohms.

3. from previous experimental data, the predicted resonator unloaded Q factor will be approximately 250.

4. the capacitive gap capacitor is 0.08pF, and requires

a microstrip gap width of 25 μm.

5. the coupling capacitor is 0.045pF, and requires a gap width of 50 μm.

6. the value of test capacitance should be approximately 1pF.

7. the resonant frequency, without the test capacitor in the circuit, will be approximately 11.8 GHz, and with the test capacitor inserted, will be approximately 8.6 GHz.

5.5 Conclusions.

In this chapter, a detailed analysis of the design of the resonator for the measurement of the characteristics of overlay capacitors, has been described, and the main features of the resulting resonator are summarised in section 5.4.8.

The relevant equations for the conditions at resonance have also been derived in section 5.4.5, which enable the test capacitor Q factor and capacitance to be determined.

Three features of the measurement technique have, as yet, not been discussed. These are;

1. the method of construction of the resonant line and the test capacitor, so that measurements can be made both with, and without, the test capacitor as an inherent part of the resonant line, without using bonding techniques.

2. the separation of the measured capacitor Q factor into the electrode Q and the dielectric Q factors.

3. the exact measurement procedure adopted, using the resonator technique described above, to determine the characteristics of the test capacitor.

In the following chapter, theories will be presented

which enable the subdivision of the capacitor Q factor into the constituent elements of dielectric and electrode Q factors.

In Chapter 7, the method of construction of the test capacitor and the resonant line will be discussed, and processing techniques adopted to improve the component performance, and to simplify the manufacturing procedure, will be described.

In Chapter 8, the exact measurement procedure adopted for the determination of the capacitor parameters from the microwave measurements will be described, and in Chapter 9, the results of measurements performed on microwave overlay capacitors will be discussed.

6. CAPACITOR IMPEDANCE ANALYSIS.

6.1 Introduction.

In the preceding chapter, a measurement technique was described for the determination of the properties of microwave overlay capacitors which could be represented by the simple equivalent circuit of figure 6.1. From these measurements it was shown that the following parameters could be calculated;

1) the effective capacitance C*, where $C^* = \frac{C}{1 - \omega^2 C L'_s}$ 6.1

2) the effective Q factor Q*, where $\frac{1}{Q^*} = \frac{1}{Q^*_E} + \frac{1}{Q^*_D}$ 6.2

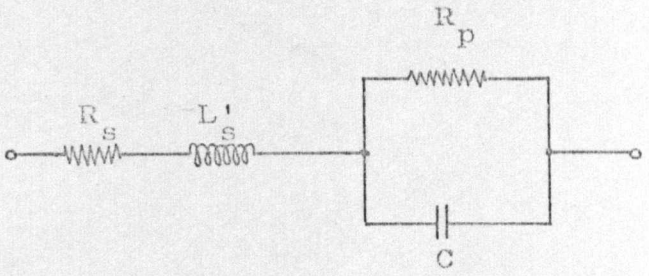
where $Q^*_D = \frac{C}{C^*} Q_D$ is the effective dielectric Q factor 6.3

and $Q_D = \omega C R_p$ is the actual dielectric Q factor

and $Q^*_E = \frac{1}{\omega C^* R_s}$ is the effective electrode Q factor 6.4

Although the measured parameters, C* and Q*, are fundamentally extremely valuable as they represent the capacitance and Q factor of practical microwave capacitors, including the effects of the necessary feeder systems, no information can be determined from these parameters concerning the dielectric constant, or the relative contributions to the capacitor loss, of the electrodes and diclectric respectively.

In this chapter, therefore, equations are derived for the electrode resistance, R_s, and the electrode inductance, L'_s, for several different electrode configurations, and these equations will, in turn, permit the evaluation of the electrode and dielectric Q factors and the dielectric constant from the data obtained using the measurement technique of Chapter 5.



R_s = electrode resistance
L'_s = electrode inductance
R_p = dielectric resistance
C = actual capacitance

figure 6.1 Equivalent circuit of a test capacitor.

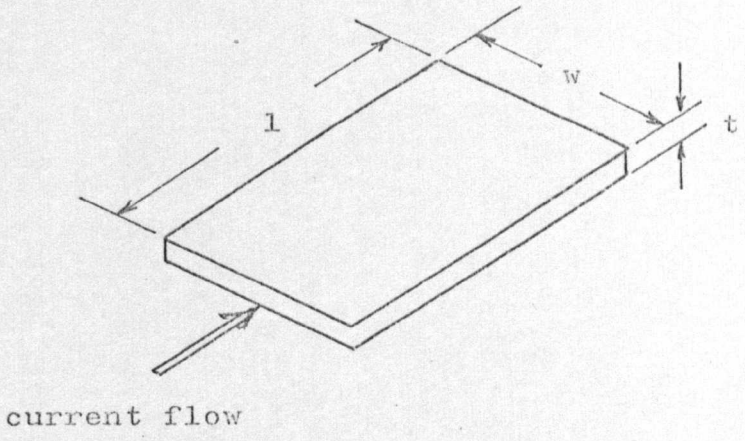


figure 6.2 Rectangular conductor.

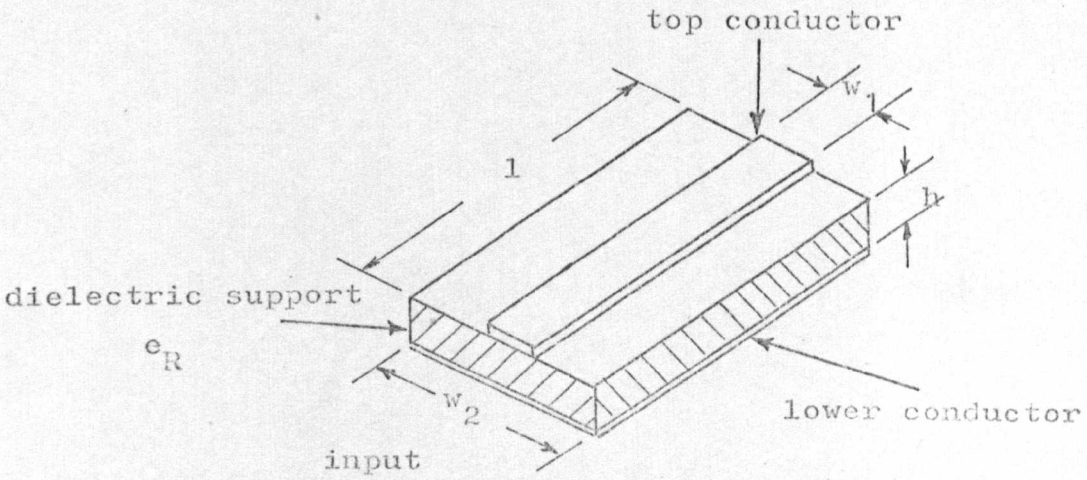


figure 6.3 Short series section of transmission line.

The theoretical analyses described also provide valuable information for the design of microwave overlay capacitors with respect to the choice of capacitor materials, capacitor configuration, electrode thickness and electrode aspect ratio (i.e. $\frac{\text{width}}{\text{length}}$).

6.2 Inductance and resistance of a transmission line.

In the evaluation of the characteristics of the electrodes of the overlay capacitors, the properties of two common circuit configurations are required. These are;

1) the resistance of a rectangular conductor (figure 6.2) of length, l, and thickness, t, in which the current is uniformly distributed as a function of width, w.
2) the inductance of a short series section of transmission line (figure 6.3) of length, l, and conductor widths, w_1 and w_2, supported by a substrate of thickness, h, and dielectric constant, e_R.

The general characteristics of these components are determined at this stage, and referred to, as necessary, in the sections to follow.

6.2.1 Resistance of a rectangular conductor.

The resistance of the rectangular conductor of figure 6.2 is

$$R = R_s \frac{l}{w} \quad \text{ohms} \qquad 6.5$$

where R_s is the surface resistivity in ohms/□ .

For an infinitely thick conductor[159]

$$R_s = \frac{1}{\sigma\delta} \quad \text{ohms/□} \qquad 6.6$$

where σ is the microwave conductivity of the conductor material, and δ is the skin depth. For relatively thin conductors[7] ($t \leq 2.5$ skin depths), the effective surface resistivity, (R_s'), is

$$R_s' = \frac{\sinh \frac{2t}{\delta} + \sin \frac{2t}{\delta}}{\cosh \frac{2t}{\delta} - \cos \frac{2t}{\delta}} \cdot \frac{1}{\sigma\delta} \quad \text{ohms/□} \qquad 6.7$$

A plot of $\frac{R_s'}{R_s}$ as a function of $\frac{t}{\delta}$ is given in figure 6.4, which indicates that for minimum conductor resistance, the ratio of conductor thickness to skin depth, $\frac{t}{\delta}$, should be 1.57 (= $\pi/2$). For film thicknesses greater than 2.5 skin depths, $\frac{R_s'}{R_s} = 1$.

The resistance of a rectangular conductor (figure 6.2), with $\frac{t}{\delta} \leq 2.5$, is then

$$R = R_s' \frac{1}{w} = \frac{1}{\sigma\delta} \frac{\sinh \frac{2t}{\delta} + \sin \frac{2t}{\delta}}{\cosh \frac{2t}{\delta} - \cos \frac{2t}{\delta}} \frac{1}{w} \quad \text{ohms.} \qquad 6.8.$$

6.2.2 Inductance of a short section of transmission line.

For a short series section of transmission line (figure 6.3), in which the resistance per unit length and the conductance per unit length are negligible compared to the capacitance per unit length, C, and the inductance per unit length, L, then the characteristic impedance, Z, is given by 160

$$Z = \sqrt{\frac{L}{C}} \qquad 6.9$$

and the velocity of propagation down the line is

$$v = \frac{1}{\sqrt{LC}} \qquad 6.10$$

Rearranging equations 6.9 and 6.10 for the inductance per unit length, we obtain

$$L = \frac{Z}{v} \quad \text{H/metre} \qquad 6.11$$

where the impedance is calculated using equations 3.1 - 3.3, and equation 3.5.

The resulting variation of the inductance per unit length of transmission line, as a function of the ratio of line width to substrate thickness ($\frac{w}{h}$), is given in figure 6.5.

Figure 6·4

Theoretical plot of the ratio of effective surface resistivity to surface resistivity as a function of the film thickness in skin depths

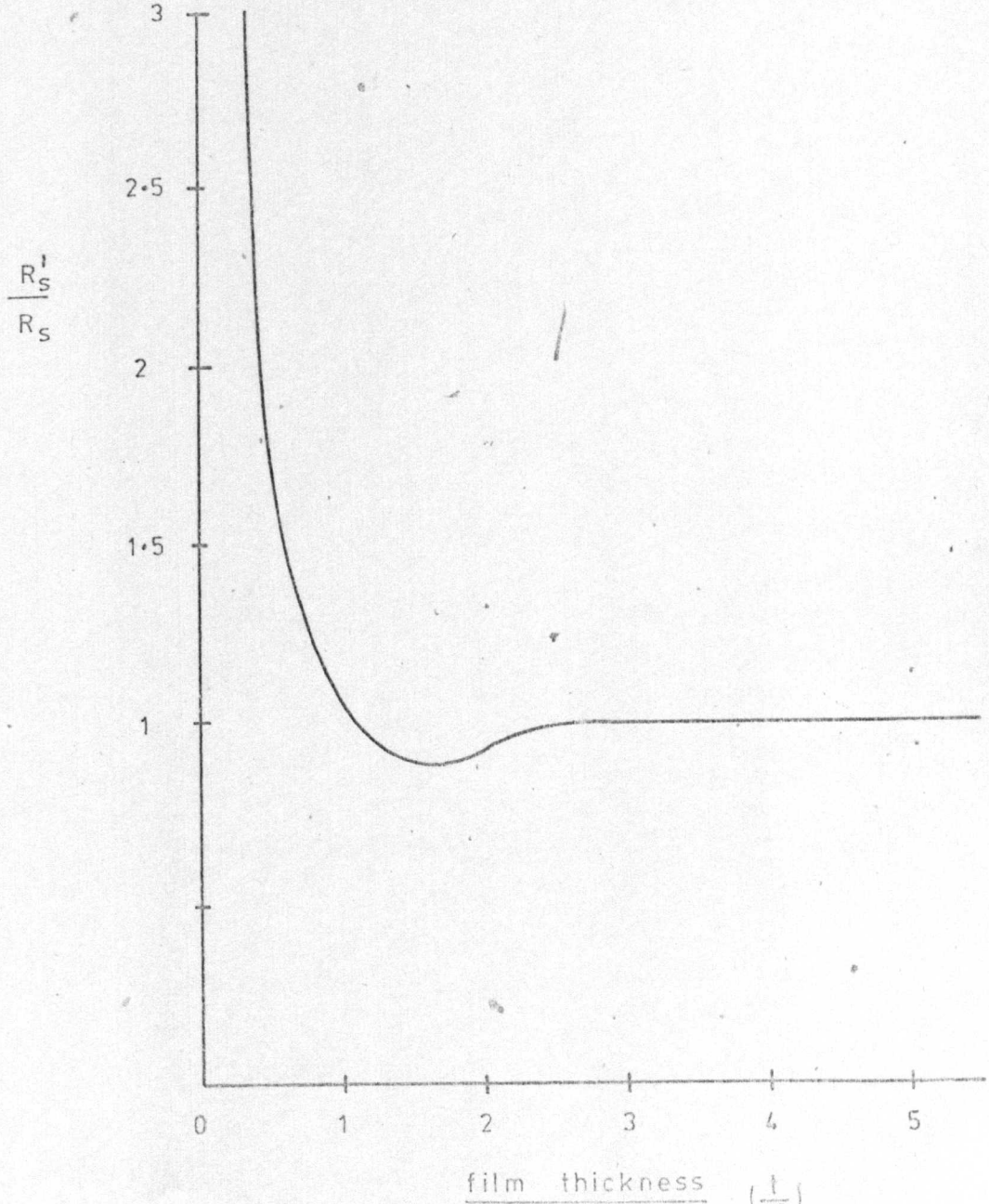
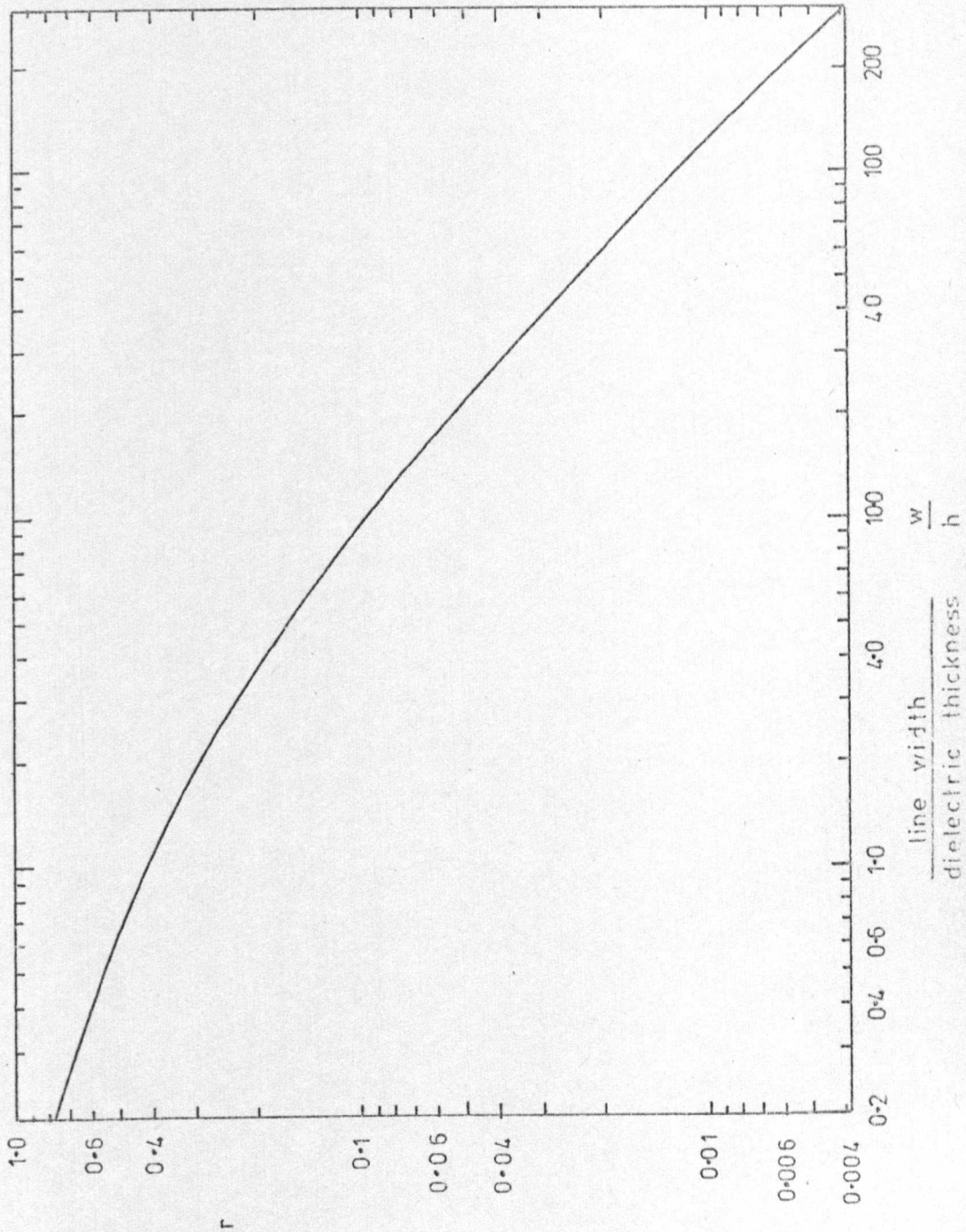


Figure 6·5

Theoretical plot of the inductance per unit length of microstrip line, as a function of the ratio of the $\frac{\text{line width}}{\text{substrate thickness}}$.

From equation 6·11. 2D capacitor configuration.



6.3 Impedance of the 2D capacitor configuration.

The simplest and most common configuration for microwave overlay capacitors, is that shown in figure 6.6. This particular configuration will be analysed in detail as it clearly defines the fundamental factors which are critical in the design of microwave overlay capacitors, and which must be carefully controlled if capacitors with the desired performance are to be reliably produced.

It is also a relatively simple procedure, to determine the characteristics of the capacitor configuration used in the measurement technique described in Chapter 5, from this basic configuration.

For the capacitor configuration shown in figure 6.6, the current is fed into, and removed from, one edge of the capacitor alone. Then, assuming

1) the dielectric electric field is confined entirely to within the dielectric, and is normal to both electrodes, i.e. there is no fringing capacitance,

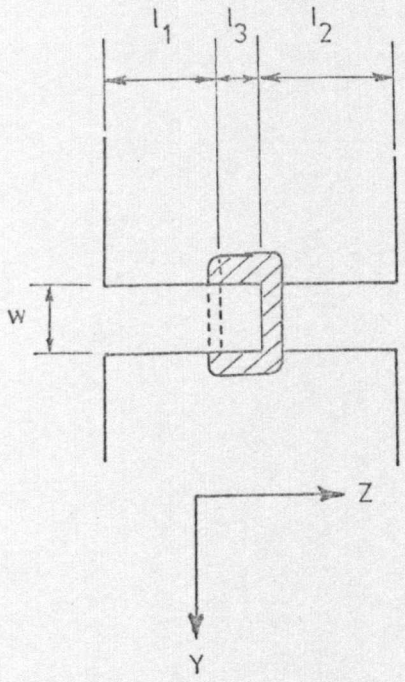
2) the electrodes are perfect conductors and are infinetely thin,

3) the voltage and current distributions at the input and output of the capacitor, are invariant in the y direction, i.e. there is no skin effect,

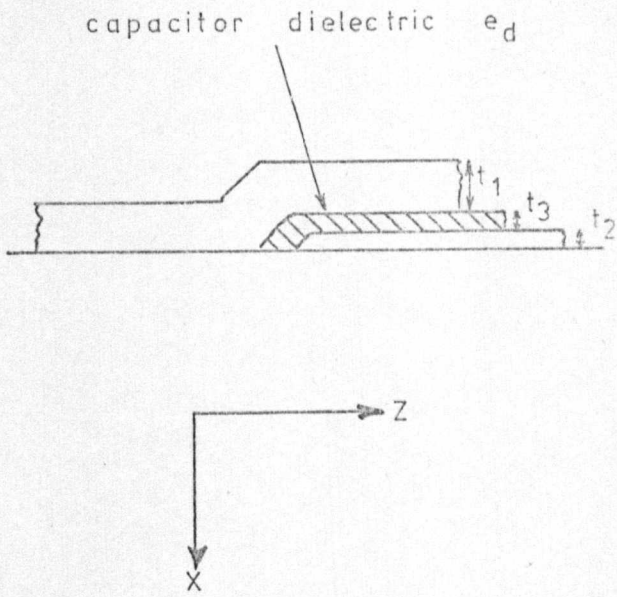
then, for the electrodes, the current can only exist in the z direction, and for the dielectric, the current flow can only exist in the x direction. The current flow in the capacitor is then only in two dimensions (2D), and the capacitor is denoted as the 2D configuration.

Having accepted these basic current flow directions, consider the effect on the current distribution and current flow, if the electrodes have a finite thickness.

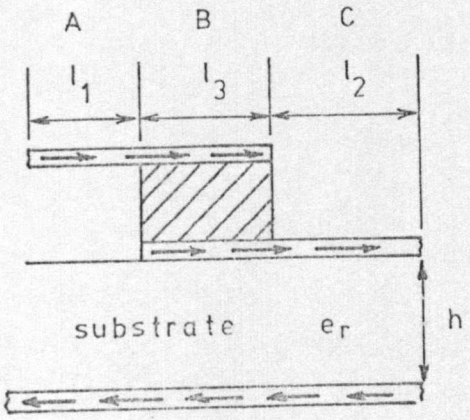
If, in the first instance, the electrode thickness is considerably less than 1 skin depth, then the current flow in the electrodes and feeders, is, to all intents and purposes, uniformly distributed as a function of thickness,



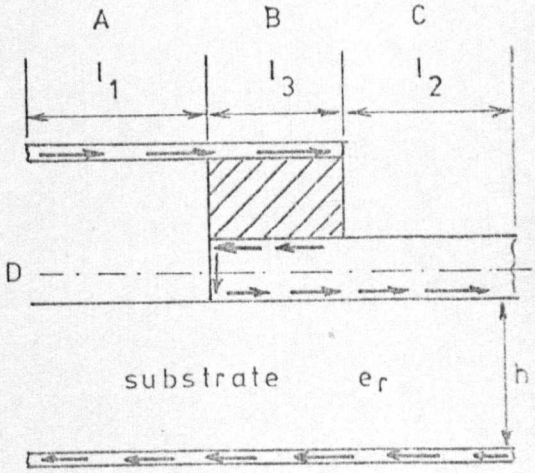
(a) capacitor plan view



(b) capacitor cross-section



(c) thin lower electrode



(d) thick lower electrode

Figure 6·6 2 D capacitor configuration

and the current flow of figure 6.6.c results.

If, on the other hand, the electrode thickness is very much greater than 1 skin depth, the current distribution, as a function of the electrode thickness, will not be uniform due to the skin effect. For the electrode feeders, (figure 6.6.d, sections A and C), which, in conjunction with the substrate ground plane, form short sections of microstrip line, the current is concentrated towards the lower face of the conductor, as in the case for conventional microstrip. This is convenient for the top electrode of the capacitor, as, in any case, the current is fed into the capacitor dielectric from the lower face of that electrode.

However, the current leaving the capacitor dielectric area is fed into the upper portions of the lower electrode. To comply with the microstrip current flow discussed above, the current must be removed from the lower face of that electrode, and as a result of the high internal resistance of the thick electrode due to the skin effect, the current is prevented from flowing directly through the centre of the conductor, and it is assumed that the current flow of figure 6.6.d is adopted.

Therefore, due to the different current paths for thick and thin electrode types, a difference in the capacitor properties will result, and in the capacitor impedance analysis to follow, the capacitor properties for both thick and thin electrode types must be determined independently.

6.3.1 Thin lower electrode

The capacitor of figure 6.6.c can be divided into 4 discrete sections, and since the total capacitor length is less than $\lambda/100$, each section can be treated as comprising of lumped elements, and can be analysed independently. These four sections are

1) the input microstrip feeder (figure 6.6.c, section A)
2) the output microstrip feeder (figure 6.6.c, section C)
3) the impedance of the top and bottom electrodes and the dielectric (figure 6.6.c, section B).
4) the impedance of the capacitor, the substrate, and the ground plane (figure 6.6.c, section B).

a) The input microstrip feeder.

The resistance of the feeder of figure 6.6.a and 6.6.c is, from equation 6.8

$$R_{F1} = \mathcal{R}'_{s1} \frac{l_1}{w} \text{ ohms} \qquad 6.12$$

where $\mathcal{R}'_{s1}$ is given by equation 6.7, in which

$\sigma = \sigma_1$ is the top electrode conductivity
$\delta = \delta_1$ is the top electrode skin depth
$t = t_1$ is the top electrode thickness.

The inductance of the microstrip feeder is described by equation 6.11, and hence the total inductance is

$$L_{F1} = \frac{Z_F}{v} l_1 \text{ H} \qquad 6.13$$

where Z_F is the feeder characteristic impedance, assuming a line width of w, and a dielectric thickness of h, equal to the substrate thickness.

b) The output microstrip feeder.

The resistance of the output microstrip feeder is, from equation 6.8

$$R_{F2} = \mathcal{R}'_{s2} \frac{l_2}{w} \text{ ohms} \qquad 6.14$$

where $\mathcal{R}'_{s2}$ is given by equation 6.7, in which

$\sigma = \sigma_2$ is the lower electrode conductivity
$\delta = \delta_2$ is the lower electrode skin depth
$t = t_2$ is the lower electrode thickness

The inductance of the microstrip feeder is described by equation 6.11, and hence the total inductance is

$$L_{F2} = \frac{Z_F}{v} l_2 \text{ H} \qquad 6.15$$

where Z_F is as defined for equation 6.13.

c) The impedance of the top and bottom electrodes and the dielectric.

In this section, the impedance of the top and bottom electrodes of the capacitor, and the dielectric alone are considered, and the effects of the substrate support and the substrate ground plane on the capacitor properties are ignored. The implications of this assumption are then considered in the following section.

For the capacitor model of figure 6.7, it has been shown (Appendix 6.1), that the input impedance can be described by

$$Z_c = \frac{1}{\gamma}\left[\frac{r_1 r_2}{r_1 + r_2}\left(\gamma l_3 + \frac{2}{\sinh \gamma l_3}\right) + \frac{r_1^2 + r_2^2}{r_1 + r_2}\coth \gamma l_3\right] \quad 6.16$$

where
$$r_1 = R_1 + j\omega L_1 \quad 6.17$$
$$r_2 = R_2 + j\omega L_2 \quad 6.18$$
$$\gamma^2 = (r_1 + r_2)(G + j\omega C) \quad 6.19$$

and all other variables are defined in figure 6.7.

For short capacitor lengths ($l_3 \leq \lambda/10$), equation 6.16 can be reduced (Appendix 6.1) to

$$Z_c = \left(\frac{R_1 + R_2}{3} + j\omega\frac{L_1 + L_2}{3}\right)l_3 + \frac{1}{(G + j\omega C)l_3} \quad 6.20$$

confirming the equation of Katoh[161].

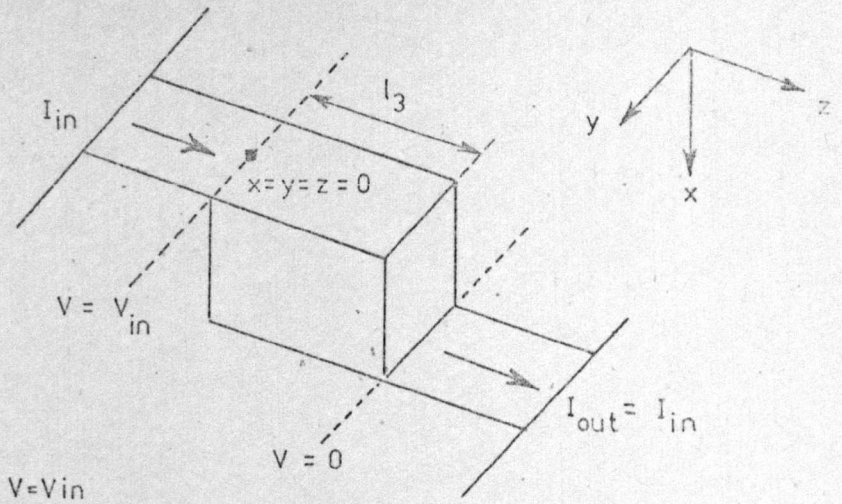
Using equation 6.8, the top electrode resistance is

$$R_1 l_3 = R'_{s1}\frac{l_3}{w} \quad 6.21$$

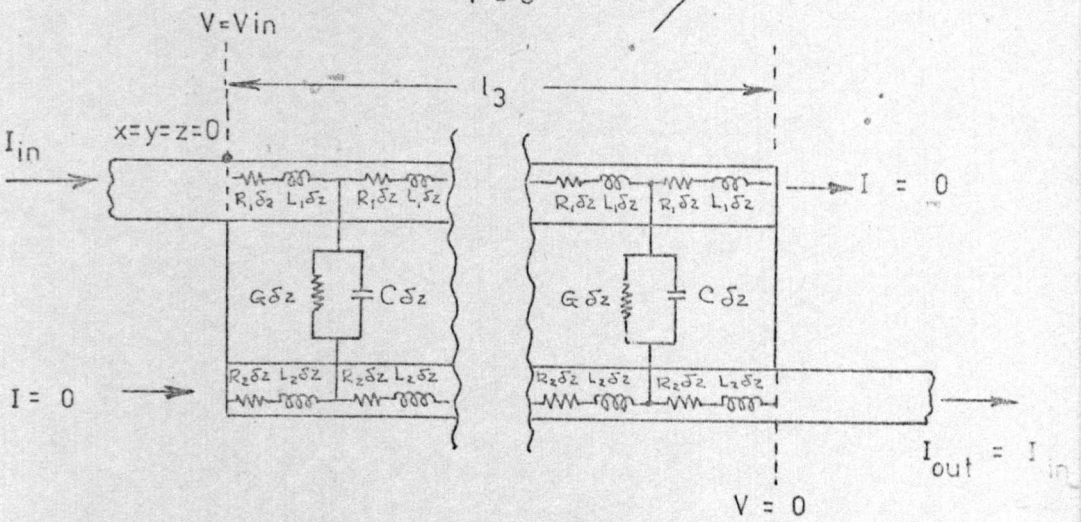
where R'_{s1} is as defined for equation 6.12.

Similarly, the lower electrode resistance is

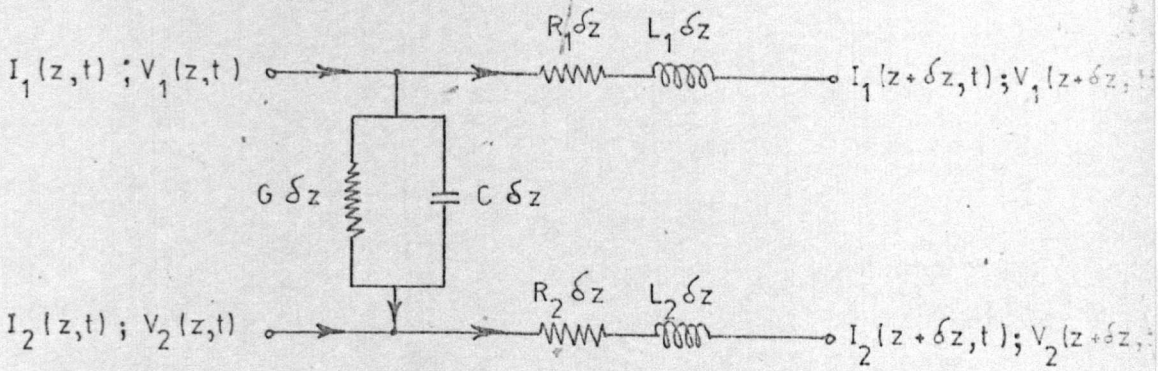
$$R_2 l_3 = R'_{s2}\frac{l_3}{w} \quad 6.22$$



(a) Schematic



(b) Mathematical model



R_1 = resistance per unit length of top electrode
R_2 = resistance per unit length of lower electrode
L_1 = inductance per unit length of top electrode
L_2 = inductance per unit length of lower electrode
C = capacitance per unit length
G = conductance per unit length

(c) Elemental length, δz, of mathematical model.

Figure 6·7 Mathematical model of overlay capacitor (2D configuration)

where $\mathcal{R}'_{s2}$ is as defined for equation 6.14.

These values for $R_1 l_3$ and $R_2 l_3$ can then be substituted into equation 6.20 to obtain the electrode resistance of the capacitor.

The total electrode inductance is, from equation 6.20

$$\frac{L_1 + L_2}{3} l_3 = \tfrac{1}{3} \text{ (total inductance/unit length)x length} \qquad 6.23$$

The total inductance per unit length is described by equation 6.11, and hence the total electrode inductance is

$$\frac{L_1 + L_2}{3} l_3 = \tfrac{1}{3} \frac{Z_c}{v} l_3 \qquad 6.24$$

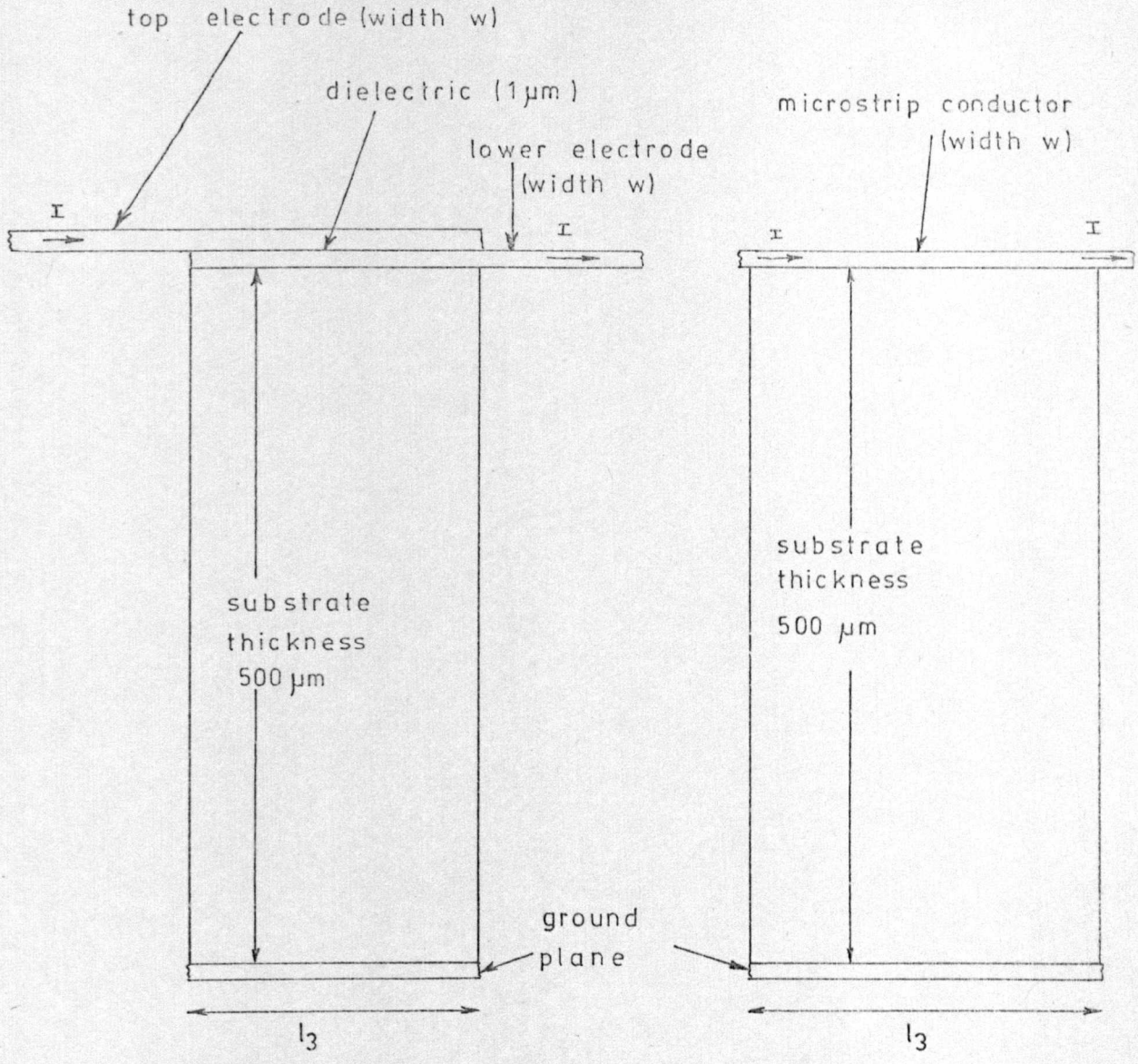
where Z_c is the characteristic impedance of the capacitor electrodes, which, to a first approximation, is described by equations 3.1 - 3.3 and 3.5, and in which the line width is w, and the dielectric thickness, t_3.

d) The impedance of the capacitor, the substrate, and the ground plane.

In addition to the inductance associated with the electrodes of the capacitor, there is inductance associated with the microstrip ground plane and the capacitor electrodes. Due to the relative magnitudes of the substrate thickness, h, and the capacitor dielectric thickness, t_3, (500 μm and 1 μm respectively), the inductance of the capacitor - ground plane system (figure 6.8), can be assumed to be identical to the inductance of a section of microstrip line, of identical width and length to that of the capacitor, and with a substrate thickness, h, of 500 μm. The capacitor - ground plane inductance is then

$$L_G = \frac{Z_F}{v} l_3 \quad \text{H} \qquad 6.25$$

in which Z_F is identical to that defined for the microstrip feeders (equation 6.13).



(a) cross section of overlay capacitor and substrate (dielectric and substrate thicknesses drawn to scale)

(b) assumed representation of the circuit of (a) for the purposes of calculating the inductance between the capacitor conductors and the microstrip ground plane.

Figure 6·8 Inductance between the capacitor electrodes and the substrate ground plane.

e) The total capacitor and feeder series impedance.

The resistance and inductance of the complete capacitor electrode and feeder system for the capacitor of figures 6.6.c and 6.1, is then the sum of the individual components described above. i.e.

$$R_s = R'_{s1}(\ell_1 + \tfrac{\ell}{3}3)\tfrac{1}{w} + R'_{s2}(\ell_2 + \tfrac{\ell}{3}3)\tfrac{1}{w} \qquad 6.26$$

$$L'_s = \frac{Z_F}{v}(\ell_1 + \ell_2 + \ell_3) + \tfrac{1}{3}\frac{Z}{v}c\,\ell_3 \qquad 6.27$$

6.3.2 Thick lower electrodes.

Capacitors with thick lower electrodes (figure 6.6.d) can be divided into 4 discrete sections, which can be analysed independently. These section are

1) the input microstrip feeder (figure 6.6.d, section A)
2) the output microstrip feeder (figure 6.6.d, section C)
3) the impedance of the top and bottom electrodes and the dielectric (figure 6.6.d, section B, above DD')
4) the impedance of the capacitor, the substrate and the ground plane (figure 6.6.d, section B, below DD').

a) The input and output microstrip feeders.

The equations describing the input and output microstrip feeder resistance and inductance are identical to those for the thin electrode configuration (equations 6.12-6.15). The resistance of the output feeder will be slightly lower for the thicker lower electrode type due to the lower surface resistivity, R'_{s2}.

b) The impedance of the top and bottom electrodes and the dielectric.

As was the case for the capacitors with thin lower electrodes, the impedance can be analysed by ignoring the existence of the microstrip ground plane. The capacitor can then be assumed to form a short section of open-circuited transmission line, of which the input impedance is

$$Z_c = Z_3 \text{ cotanh } \gamma \ell_3 \qquad 6.28$$

where $$Z_3 = \sqrt{\frac{r_1 + r_2}{G + j\omega C}} \qquad 6.29$$

and r_1, r_2 and γ are as defined in equations 6.17-6.19.

For short capacitor lengths (i.e. $l_3 < \lambda/10$), equation 6.28 can be reduced to

$$Z_c = Z_3 \left(\frac{1}{\gamma \ell_3} + \frac{\gamma \ell_3}{3}\right) \qquad 6.30$$

which can be simplified to

$$Z_c = \left(\frac{R_1 + R_2}{3} + j\omega \frac{L_1 + L_2}{3}\right)\ell_3 + \frac{1}{(G + j\omega C)\ell_3} \qquad 6.31$$

From a comparison of this equation with equation 6.20, it can be seen that for short capacitor lengths, the input impedance is identical for both the thin and thick lower electrode types. The capacitor electrode resistance and inductance for the thick electrode configuration are therefore given by equations 6.21 - 6.24 inclusively.

c) The impedance of the capacitor, the substrate and the ground plane.

The differing current flow in the lower electrode for the thick electrode capacitor type, introduces an additional resistance, which is

$$R_L = \mathcal{R}'_{s2} \frac{\ell_3}{w} \qquad 6.32$$

As in the case of the thin electrode type, there is inductance between the capacitor electrodes and the microstrip ground plane. Since the total nett current in the capacitor electrodes, in the direction of capacitor current flow, is identical for capacitors with either thick or thin lower electrodes (figures 6.6.c and 6.6.d), and since the electrode and dielectric thicknesses are very much less than the substrate thickness, then the inductance between the capacitor electrodes and the substrate ground plane, is identical for both capacitor types. The inductance is then given by equation 6.25.

d) The total capacitor and feeder impedance.

The total electrode and microstrip feeder impedance for capacitors with thick lower electrodes (figure 6.1 and 6.7.d) is then

$$R_s = \mathcal{R}'_{s1}\left(\ell_1 + \frac{\ell_3}{3}\right)\frac{1}{w} + \mathcal{R}'_{s2}\left(\ell_2 + \frac{4}{3}\ell_3\right)\frac{1}{w}$$

$$L'_s = \frac{Z_F}{v}(\ell_1 + \ell_2 + \ell_3) + \frac{1}{3}\frac{Z_c}{v}\ell_3$$

6.3.3 Design considerations for the 2D configuration.

From equations 6.1 to 6.4, it can be seen that

1) an increase in the electrode inductance, L'_s, increases the variation of the effective capacitance, C^*, with frequency. If, for example, the ratio of the inductive reactance to the capacitive reactance, $\omega^2 L'_s C$, is 0.1, then the effective capacitance, C^*, will change by approximately 8% as the frequency is swept from dc to 12 GHz.
2) an increase in the electrode inductance, increases the effective capacitance, C^*, and hence decreases the effective dielectric Q factor, Q^*_D, and the effective electrode Q factor, Q^*_E, and hence decreases the effective capacitor Q factor, Q^*. If the ratio of inductive reactance to capacitive reactance is 0.1, then the effective Q factor will be reduced by 10%.
3) an increase in the electrode resistance, R_s, decreases the electrode Q factor, and hence decreases the effective capacitor Q factor.

Therefore, to minimise the variation of the effective capacitance, C^*, with frequency, and to minimise reduction in the capacitor Q factor, both the electrode resistance and the electrode inductance should be reduced to the absolute minimum, and methods of achieving this are discussed in the following sections.

Electrode resistance.

It is evident from equation 6.26 that the microstrip feeder lengths, ℓ_1 and ℓ_2, contribute more to the total resistance per unit length, than does the electrode length, ℓ_3. The feeder lengths should therefore be kept to the absolute minimum, and should be much shorter than the electrode length, ℓ_3. Assuming this to be the case, the total series resistance, R_s, is then determined predominantly by the electrode resistance.

Electrode thickness.

The physical nature of the overlay capacitor, (figure 6.6.b) implies no physical limitation on the thickness of the top electrode, and it should be selected to minimise the resistance. i.e. from figure 6.4, the optimum thickness is 1.57 skin depths.

The lower electrode thickness, on the other hand, is restricted by the necessity of obtaining a good dielectric overlay, without introducing pinholes or low voltage breakdown, and is generally restricted to a thickness considerably less than the top electrode thickness. It will be observed from figure 6.4, that the lower electrode sheet resistance, R'_{s2}, will then be greater than the top electrode sheet resistance, R'_{s1}, and therefore, from equation 6.26, the lower electrode will contribute more to the total electrode loss than does the top electrode.

To reduce the resistance of the lower electrode, the thickness may be increased. However, it has been shown, (equation 6.33), that if the thickness is considerably increased, so that it is very much greater than a skin depth, the resistance will in fact increase due to the change in current flow, as indicated in figure 6.6.d.

In figure 6.9 it is indicated that the optimum thickness for the lower electrode is approximately 1 skin depth, as below this thickness, the losses increase rapidly, and above this, the additional benefits from a further increase in thickness rapidly diminish.

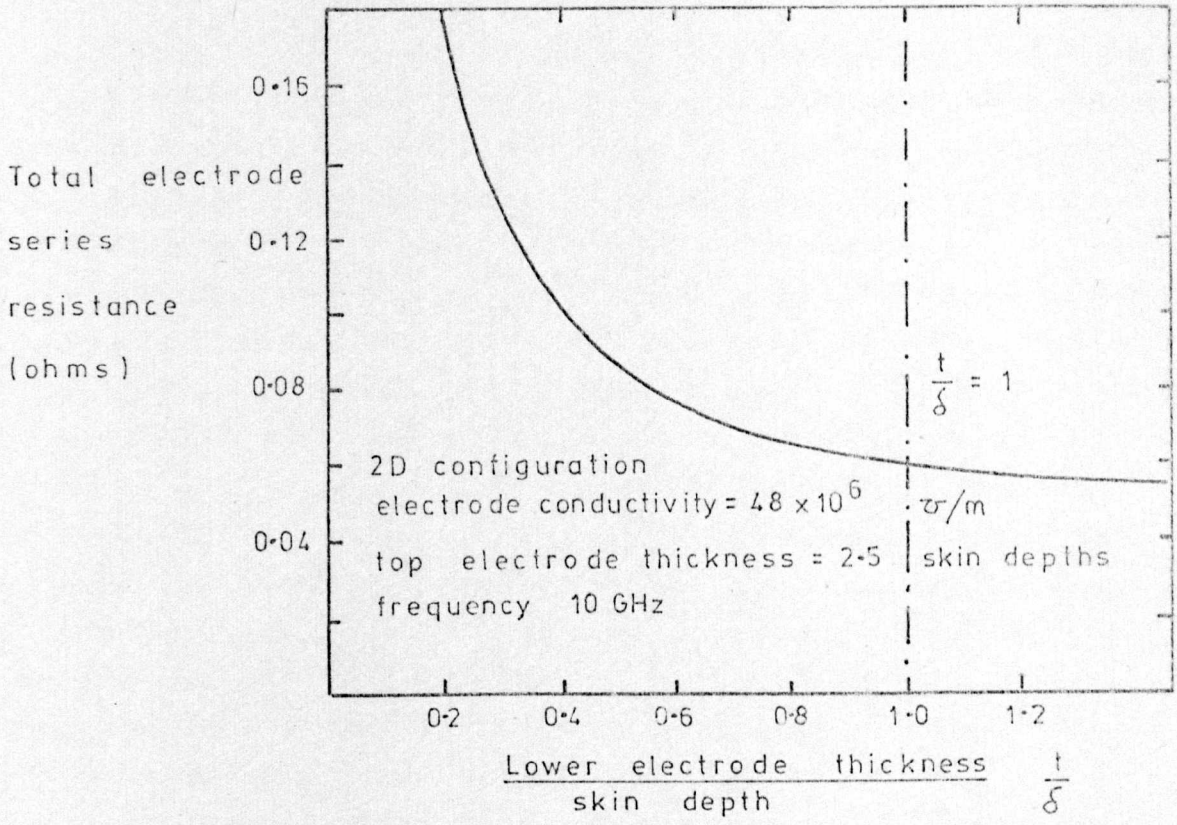


Figure 6·9 Theoretical variation of the total electrode resistance as a function of the lower electrode thickness.

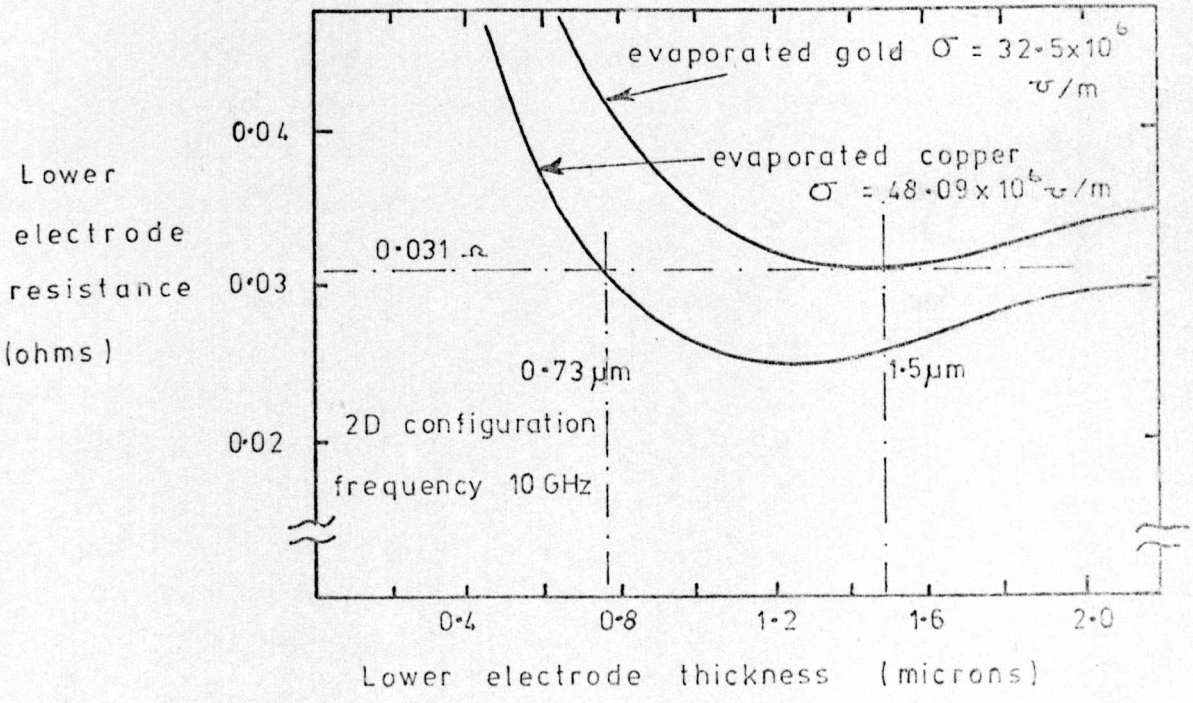


Figure 6·10 Theoretical variation of the lower electrode resistance as a function of the lower electrode thickness for copper and gold electrodes.

Electrode material.

If a material with a higher conductivity is used for the electrodes, then the electrode resistance will be reduced, as is indicated by equation 6.8. There are, however, additional, less obvious advantages to be gained by using a high conductivity material for the lower electrode.

If, for example, (figure 6.10), the lower electrode resistance is maintained constant at say, 0.031 ohms, then, using a gold electrode, the required electrode thickness is 1.5 μm. If, on the other hand, copper, with its higher conductivity, is used as the electrode material, then the required thickness is only 0.73 μm. This thinner electrode can then permit the use of a thinner dielectric layer, which in turn leads to higher capacitance per unit area, reduced dielectric deposition time, and, a factor which will be established in the sections to follow, a reduction in the parasitic electrode inductance.

Therefore, there are significant advantages to be gained by using copper in preference to gold, or any other lower conductivity material, for the lower electrodes of overlay capacitors.

Capacitor aspect ratio.

The importance of the capacitor aspect ratio, (i.e. $\frac{\text{width}}{\text{length}}$), in determining the electrode Q factor, is indicated in figure 6.11. This figure plots the electrode Q factor, (neglecting the effects of the microstrip feeders), as a function of the capacitor aspect ratio, for selected values of the capacitance. Also indicated in the figure is the upper acceptable limit for the aspect ratio. This is assumed to occur when the capacitor width is equal to $\lambda/10$, as for greater widths, the distributed effects increase in magnitude, and the capacitor cannot be treated as a truly lumped component. The upper limit for the aspect ratio is then a function of the capacitance, the capacitor dielectric thickness and dielectric constant, the substrate dielectric constant, and the frequency.

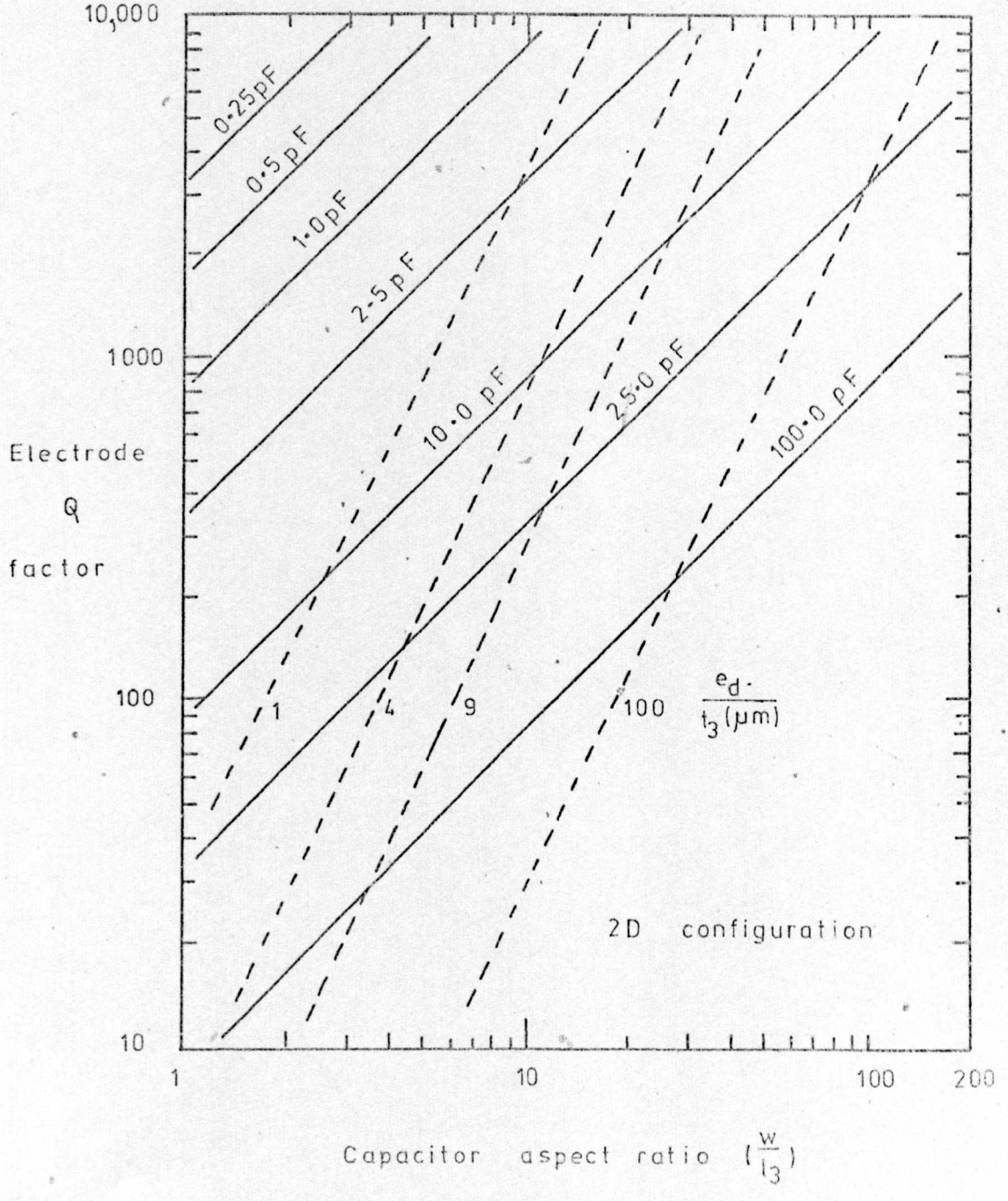
Figure 6·11

Electrode Q factor as a function of the capacitor aspect ratio for selected values of capacitance at 10GHz

top electrode ≡ 1·8 skin depths of bright copper plate
$\sigma = 48 \times 10^6$ ℧/m

lower electrode ≡ 1 skin depth of evaporated copper
$\sigma = 48{\cdot}09 \times 10^6$ ℧/m

– – – – – – upper limit of aspect ratio determined when $w = \frac{\lambda}{10}$ and assuming a frequency of 10 GHz and quartz substrates



From figure 6.11 it can be seen that for low value capacitors ($\approx$1pF), using 1 μm of silicon dioxide as dielectric (i.e. $e_d/t_{3(\mu m)} \approx 4$), electrode Q factors of approximately 1000 can be achieved, at 10 GHz, using capacitor aspect ratios close to unity.

For high value capacitors ($\approx$100pF), however, using a similar thickness of silicon dioxide, electrode Q factors will be limited to approximately 10 due to the restriction placed on the upper limit of aspect ratio.

The Q factor can only be increased by significantly increasing the e_d/t_3 ratio, or by increasing the upper limit of aspect ratio by using a substrate with a lower dielectric constant. This latter factor therefore emphasises the advantages of using quartz in preference to higher dielectric constant materials (e.g. sapphire) for L.E. M.I.C. substrates.

Any increase in the e_d/t_3 ratio achieved by reducing the dielectric thickness, t_3, is generally minimal due to the introduction of pinholes in the dielectric, and a lowering of the breakdown voltage.

The electrode Q factor for high value capacitors can only be significantly improved, therefore, by utilising high dielectric constant materials ($e_d \approx 100$), and such materials, with the necessary low loss at microwave frequencies, are, as yet, unavailable.

If it is assumed that the lowest tolerable electrode Q factor at 10 GHz, is 100, then for capacitors on quartz substrates, using the most common microwave dielectric materials of silicon dioxide and alumina, it is estimated that the largest practical capacitor values will be approximately, 30pF and 45pF, respectively.

Electrode inductance.

The total inductance of the capacitor electrodes and feeders is given by equation 6.27, and it can be seen by comparison with equation 6.34, that the inductance is independent of the lower electrode thickness.

It can be observed from figure 6.5, that for the capacitor and substrate dimensions used in this thesis,

(i.e. $w = 200\ \mu m$, $h = 500\ \mu m$, $t_3 = 1\ \mu m$), the first term in equation 6.27 is more than 300 times greater than the second term, and hence the total electrode inductance can be approximated by

$$L'_s = \frac{Z_F}{v}(l_1 + l_2 + l_3) \qquad 6.35$$

Therefore, to minimise the electrode inductance, the feeder lengths, l_1 and l_2, and the capacitor length, l_3, should be kept to the absolute minimum.

To give an indication of the capacitor dimensions required to maintain the electrode inductance to an acceptable level, a plot is given in figure 6.12, of the capacitor width as a function of the capacitance, for selected values of the ratio of dielectric constant to dielectric thickness, for an $\frac{\text{inductive reactance}}{\text{capacitive reactance}}$ ratio of 0.1. Also indicated in this figure, is the maximum permissible value of capacitor width (= $\lambda/10$), at 10 GHz, for both quartz and sapphire substrate materials.

This figure emphasises the advantages of using quartz in preference to other higher dielectric constant materials as the substrate support, and also emphasises the importance of a high ϵ_d/t_3 ratio to maintain a low inductive reactance. The high ϵ_d/t_3 ratio, as indicated previously, can only be reliably achieved by using high dielectric constant materials for the dielectric films.

In the complementary diagram of figure 6.13, it is shown that for typical quartz and alumina capacitor dimensions, (i.e. $\epsilon_d/t_3(\mu m)$ = 4 and 9 respectively), assuming that the maximum acceptable inductive reactance/capacitive reactance ratio is 10%, then the practical upper limit of capacitance, using quartz substrates at 10 GHz, is approximately 2.5pF and 4pF, for quartz and alumina capacitor dielectric materials respectively.

The limiting factor determining the upper practical limit of capacitance, is then the parasitic electrode inductance.

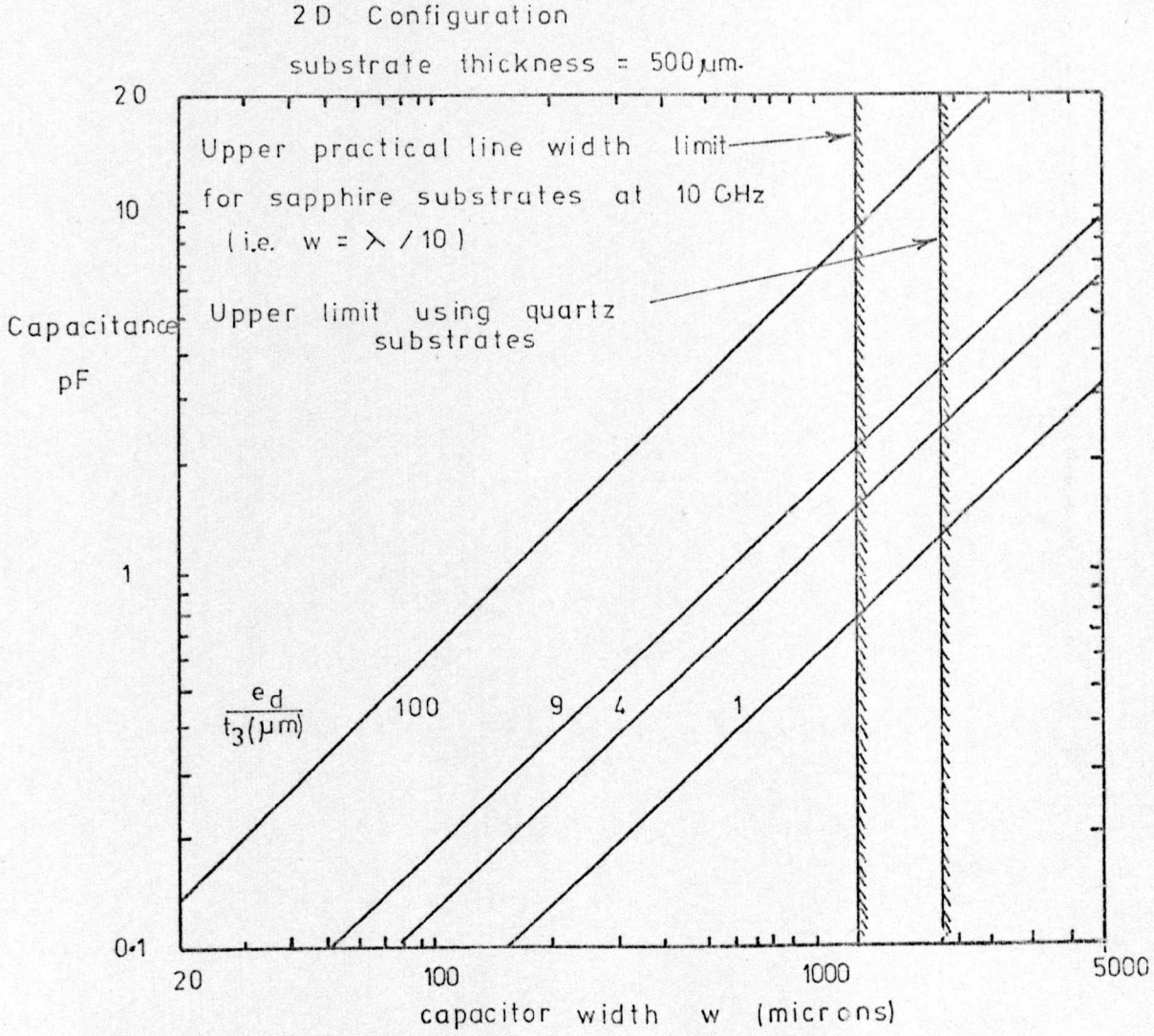


Figure 6·12 The required capacitor width as a function of the capacitance, to maintain the ratio of inductive reactance to capacitive reactance at 0·1, for selected values of capacitor dielectric constant / dielectric thickness (e_d/t_3)

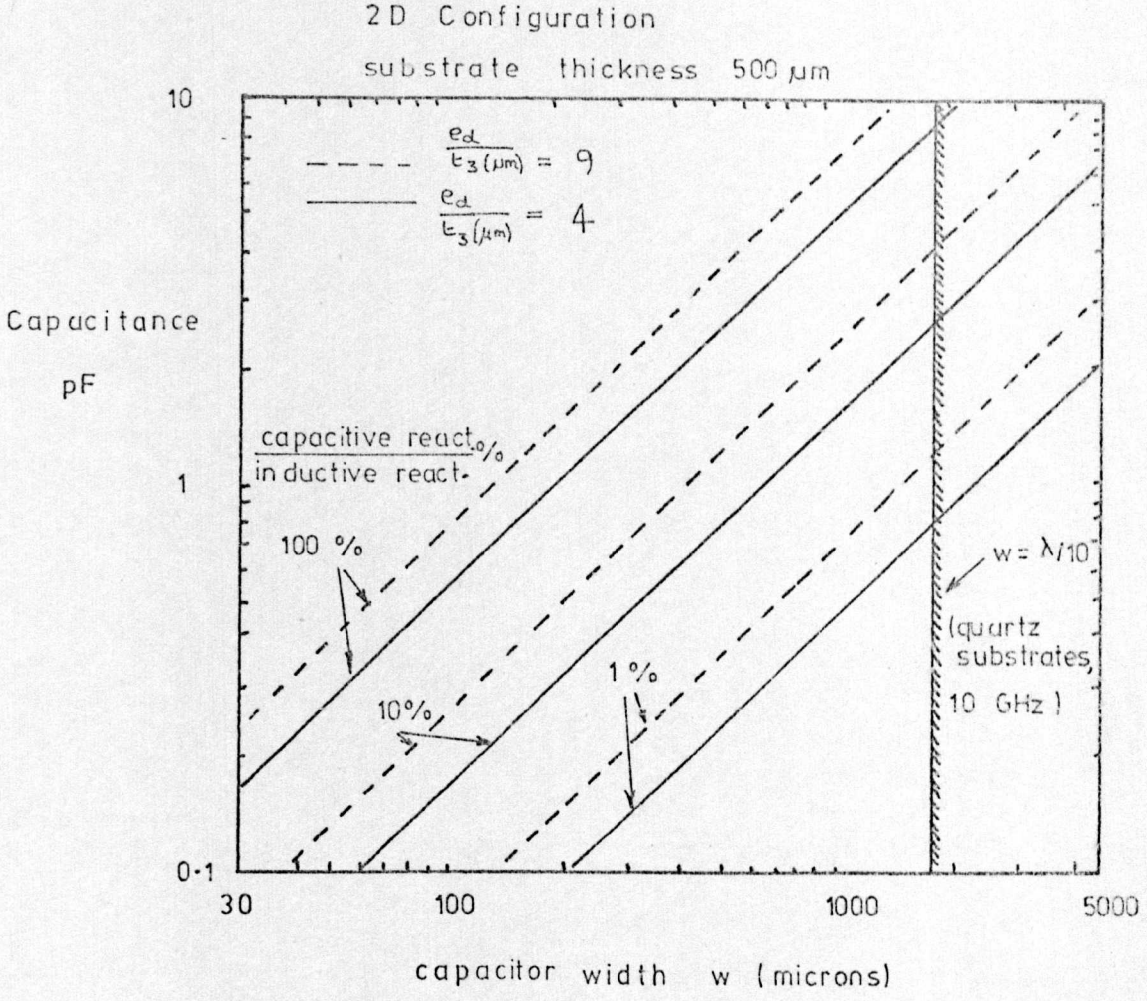


Figure 6·13 Capacitor width as a function of the capacitance to obtain selected values of $\frac{\text{inductive reactance}}{\text{capacitive reactance}}$, for $\frac{e_d}{t_3(\mu m)} = 4$ and 9.

6.4 Impedance of the 3D capacitor configuration.

An alternative electrode arrangement to the 2D configuration, is the 3D configuration shown in figure 6.14, in which the current is fed into one edge of the capacitor, and is removed from three edges.

Special consideration was given to this particular configuration, as it was adopted for the capacitors to be measured using the resonator technique described in Chapter 5.

In figure 6.14, assuming

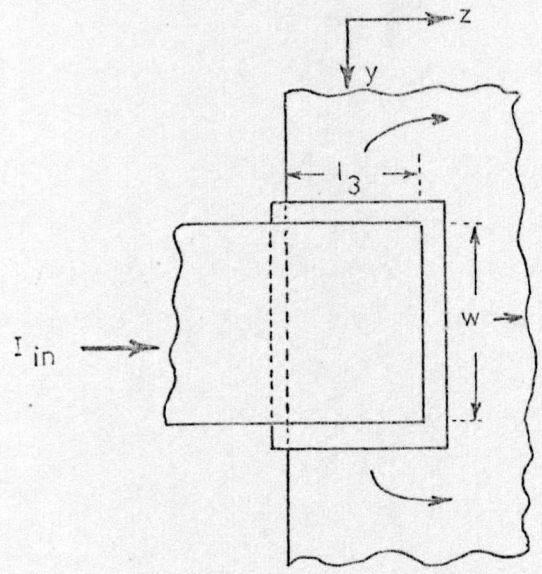
1) the electric field is confined to entirely within the dielectric area, and is normal to both electrodes, (i.e. there is no fringing capacitance),
2) the electrodes are perfect conductors and are infinitely thin,
3) the voltage and current distributions at the input are invariant in the y direction, and at the output are invariant across the three output edges (i.e. there is no skin effect),

then the current flow in the dielectric can exist only in the x direction, and in the electrodes can exist only in the y and z directions. There is, therefore, current flow in 3 dimensions (3D), and the capacitor is denoted as the 3D configuration.

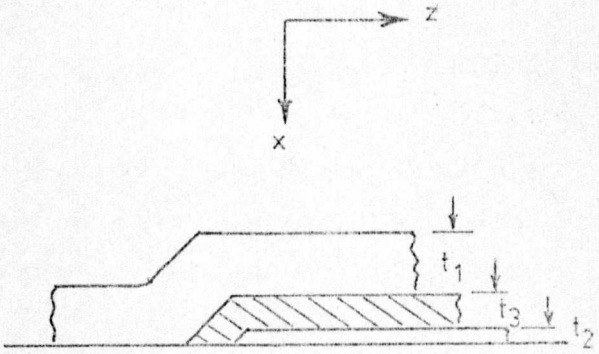
Having accepted these basic current flow directions, consider the effects of the electrodes having a small finite thickness, and a small finite inductance and resistance per unit length, such that

R_1 is the resistance per unit length of the top electrode
R_2 is the resistance per unit length of the lower electrode
L_1 is the inductance per unit length of the top electrode
L_2 is the inductance per unit length of the lower electrode
C is the capacitance per unit area
G is the conductance per unit area

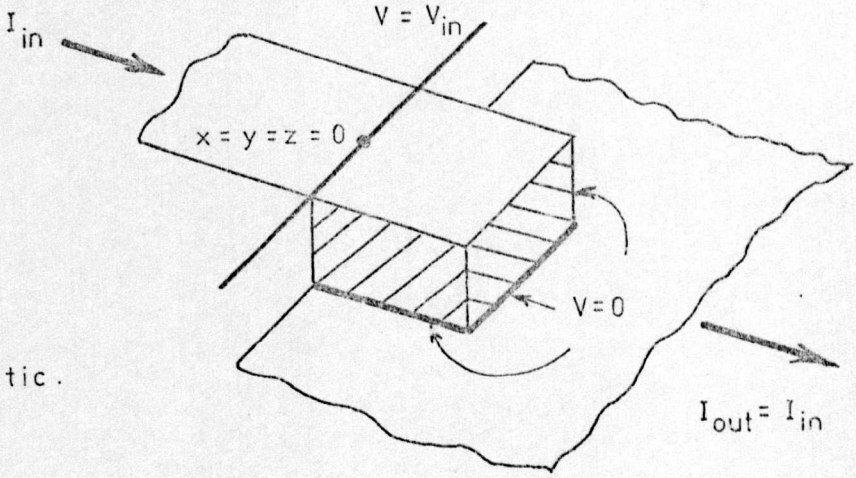
The differential equation describing the voltage distribution on the top electrode of the capacitor of figure 6.14 is then



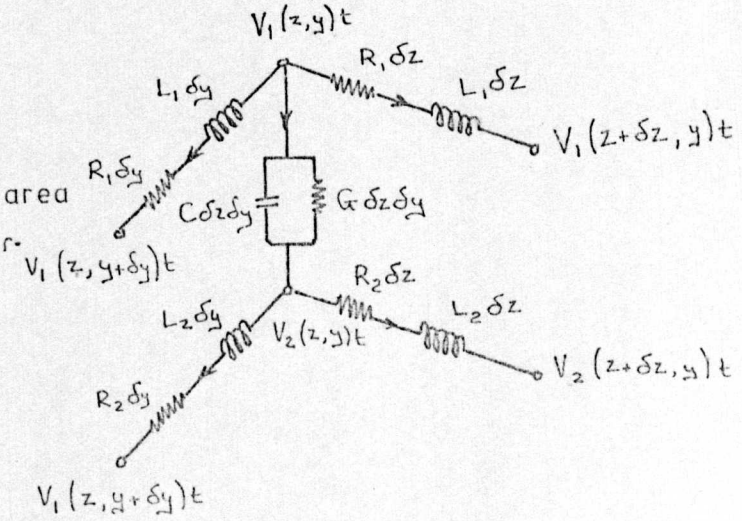
(a) plan view



(b) elevation



(c) Schematic.



(d) elemental area of capacitor

Figure 6-14 3D capacitor configuration

$$\frac{\partial^4 V_1}{\partial z^4} + \frac{\partial^4 V_1}{\partial y^4} + 2\frac{\partial^4 V_1}{\partial y^2 \partial z^2} - \gamma^2\left(\frac{\partial^2 V_1}{\partial y^2} + \frac{\partial^2 V_1}{\partial z^2}\right) = 0 \qquad 6.36$$

where $$\gamma^2 = (R_1 + j\omega L_1 + R_2 + j\omega L_2)(G + j\omega C) \qquad 6.37$$

A solution to this equation, which satisfies all the boundary conditions shown in figure 6.14.c, has so far been elusive. The capacitor input impedance was therefore determined by constructing a distributed scaled model of the microwave overlay capacitor, using conventional low frequency lumped components, and measuring the input impedance, at a relatively low frequency, by conventional r.f. measurement techniques (i.e. Q meter), as described in the following sections.

6.4.1 Scaled model measurement technique.

To simplify the construction of the scaled models, it was assumed that

1) since the parameters of most interest were the electrode resistance and the electrode inductance, the shunt resistance of the capacitor (i.e. the dielectric loss resistance) could be ignored.
2) since it has been shown (equation 6.20) that for the 2D capacitor configuration, the mathematical form of the inductive term is identical to that of the resistive term, (i.e. $\frac{\text{resistance(inductance) per unit length}}{3}$), it was assumed that a mathematical similarity would also exist for these terms in the 3D configuration. The inductance was therefore ignored in the scaled model measurements, but for the final capacitor input impedance expression, an inductive term could be included which, mathematically, would be of the same form as the resistive term.

The scaled models were therefore constructed using the unit of figure 6.15 as the basic building block, where the capacitance, C, is the capacitance per unit area, and the resistances, R_1 and R_2 are the surface resistivities of the top and bottom electrodes respectively.

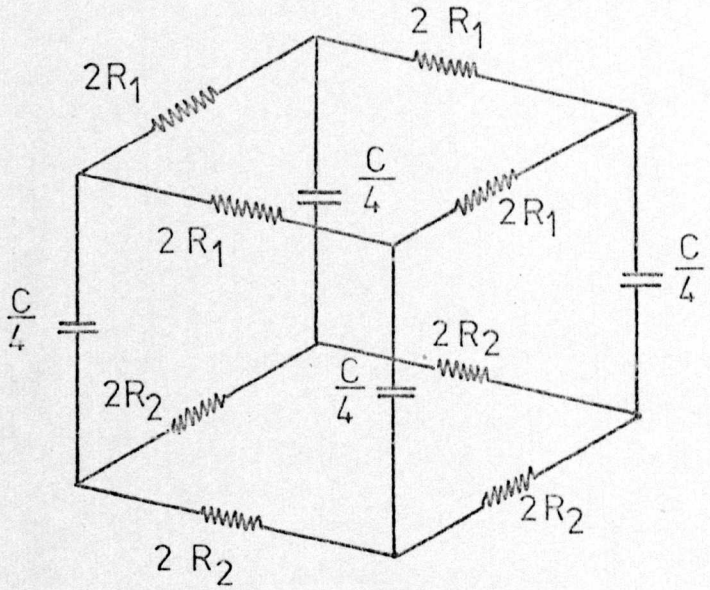


Figure 6·15 Unit cell as used in the scaled model measurements.

Model scaling factors.

The parameters evaluated from the model measurements were the capacitance, C, and the electrode series resistance, R_s, but to be of practical significance, these parameters had to be related to the corresponding parameters of an X band capacitor. This was assumed to be a 1pF capacitor operating at 10GHz.

If suffix, m, refers to the model parameters, and suffix, x, refers to the corresponding X band parameters, then

$$Q_m = \frac{1}{\omega_m C_m R_{sm}}$$

and $$Q_x = \frac{1}{\omega_x C_x R_{sx}}$$

therefore

$$Q_x = \frac{\omega_m}{\omega_x} \cdot \frac{C_m}{C_x} \cdot \frac{R_{sm}}{R_{sx}} \cdot Q_m \qquad 6.38$$

Providing, therefore, that the ratios $\frac{\omega_m}{\omega_x}$, $\frac{C_m}{C_x}$ and $\frac{R_{sm}}{R_{sx}}$ were known for each measurement, the equivalent X band capacitor electrode Q factor, Q_x, could be calculated from the measured model electrode Q factor, Q_m.

Typical X band capacitor electrode Q factors were predicted to be approximately 1000, and to increase the accuracy of measurement of the scaled model electrode resistance, the model Q factors were selected to be approximately 20. The product of the scaling factors of equation 6.38, was then 50, and the individual scaling factors were selected as indicated in the sections to follow.

Frequency scaling factor.

The model measurement frequency was chosen to be as low as possible to reduce errors due to parasitic effects, and so that the Q meter variable capacitor could be operated in the middle of its dynamic range. The selected measurement frequency was 50 kHz (which was maintained throughout the

measurements to within 0.01%). As all model measurements were referred to a 1pF capacitor at 10 GHz, the frequency scaling factor was then

$$\frac{\omega_m}{\omega_x} = 5 \times 10^{-6}$$

which was constant for all measurements.

Resistance scaling factor.

The resistor values used in the model measurements, (figure 6.15), were equal to the surface resistivities of the electrodes. The surface resistivity of the top electrode, assuming a 2.5 skin depths thick film of bright copper electroplate ($\sigma = 46.73 \times 10^6$ $\mho/m$)[7], is, from equation 6.6

$$R_1 = 0.0298\ \Omega/\square$$

The lower electrode surface resistivity, assuming a 1 μm thick film of evaporated copper ($\sigma = 48.09 \times 10^6$ $\mho/m$)[7] is, from equation 6.7

$$R_2 = 0.052\ \Omega/\square$$

Considering the frequency and capacitance scaling factors discussed above, a convenient value for the resistors used in the scaled models was of the order of 27 ohms and 47 ohms respectively, with a resulting scaling factor of

$$\frac{R_{sm}}{R_{sx}} = \frac{27}{0.027} = 1000$$

Capacitance scaling factor.

The total model capacitance is one of the measured parameters, and the exact scaling factor would, therefore, be established independently for each model.

However, assuming the other scaling factors were as discussed above, a convenient capacitor scaling factor would be approximately, 10,000, and for typical model capacitor dimensions, this assumed a basic capacitor value, C, of 1000pF,

Scaling factor summary.

From the preceding discussion, the product of the scaling factors is

$$\frac{\omega_m}{\omega_x} \cdot \frac{R_{sm}}{R_{sx}} \cdot \frac{C_m}{C_x} = \frac{5}{10^6} \cdot 10^3 \cdot \frac{C_m(\text{measured})}{1 \times 10^{-12}} = \frac{C_m(\text{pF})}{200}$$

The electrode Q factor of the equivalent 1 pF capacitor at 10 GHz, could therefore be obtained from the model electrode Q factor (Q_m), using the expression

$$Q_x = \frac{C_m(\text{pF})}{200} Q_m \qquad 6.39$$

Model measurement technique.

The capacitance and Q factor of the scaled models were measured using a Marconi Instruments Circuit Magnification Meter (type TF 1245), which, in conjunction with the series loss test jig (type TF 230), enabled the capacitance to be measured with an accuracy of $\pm 0.25\%$, and the Q factor with an accuracy of $\pm 5\%$.

The measurement technique is well documented[162], and will not therefore, be repeated at this stage.

A factor which was essential to take into account in the measurement analysis, however, was the loss resistance of the capacitors used in the model. Failure to acknowledge this resistance could lead to errors in electrode resistance of up to 100%, for model capacitors with extremely large aspect ratios.

Verification of the measurement system accuracy.

To determine the minimum number (i.e. the mesh number) of the unit cells of figure 6.15 required in the capacitor models to obtain the desired measurement accuracy (due to the model not being an accurate representation of a distributed capacitor for a small number of unit cells), measurements were initially performed on a 2D capacitor, as

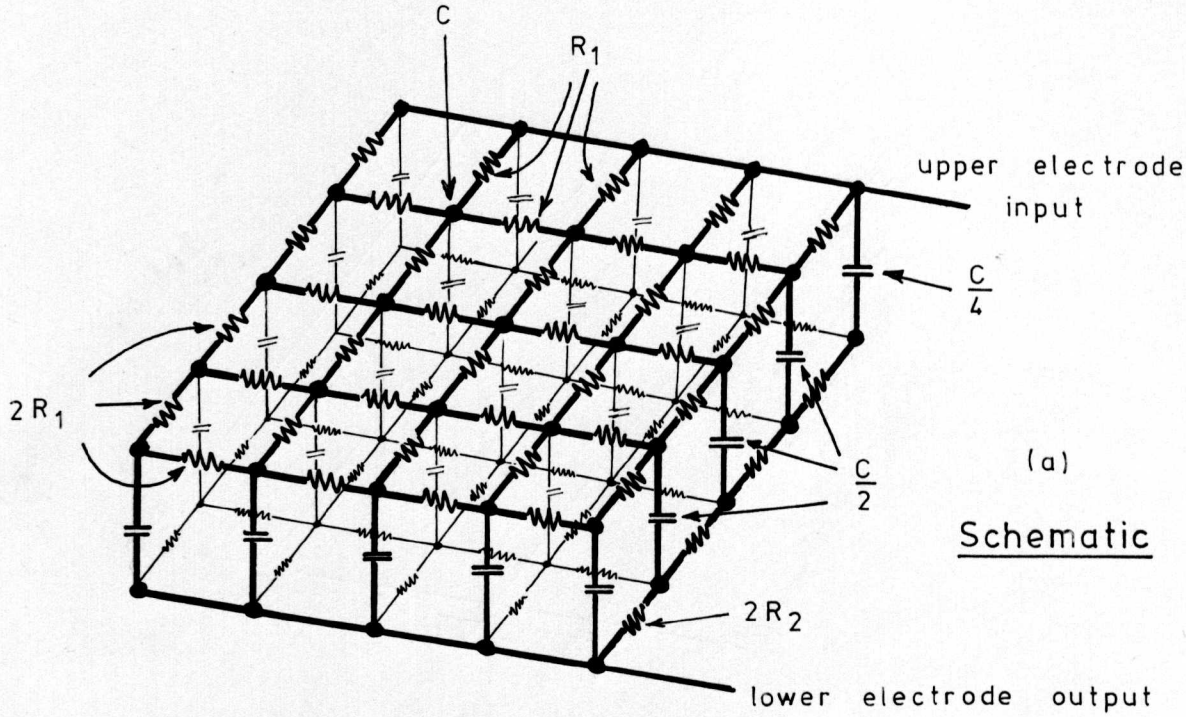
a theoretical analysis for the input impedance was already in existence (equation 6.20).

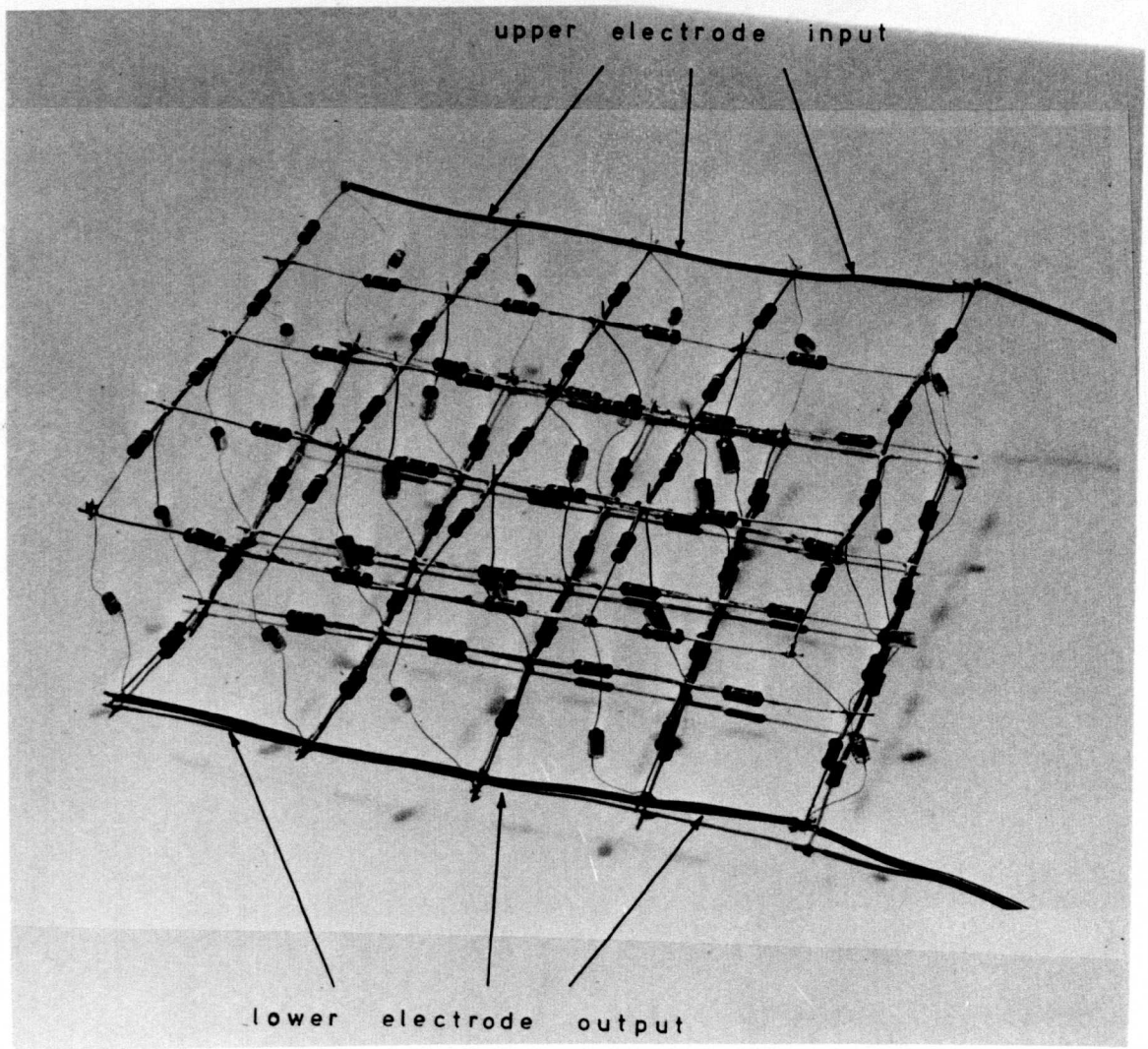
A typical 2D model capacitor, with a mesh number of 4, and an aspect ratio of 1, is shown in figure 6.16.

The series resistance of several 2D capacitor models, with aspect ratios of unity, and with varying mesh numbers, were measured as described above, and the series resistance was plotted (figure 6.17) as a function of the mesh number, and compared with the theoretical value obtained using equation 6.20. From the resulting graph it could be seen that a mesh number of 4 was sufficient to obtain results within 1.25% of the theoretical value. Therefore, for all subsequent measurements, a minimum mesh number of 4 was adopted for each capacitor model. i.e. for models with an aspect ratio of 1, the width had 4 meshes, and the length had 4 meshes; for an aspect ratio of 0.5, the width had 4 meshes, and the length had 8 meshes, etc..

Also shown in figure 6.17, are the theoretical results computed using two independent computer programs (Micro 3[163], GCAP2S[164]). It was initially considered possible to analyse all the capacitor models using one, or other, of these programs, and thus eliminate the tedious construction of the scaled models. Neither program, however, had the capacity to cope with the large number of components and nodes required for the capacitors to be analysed at a later stage in the project. For example, the smallest model (i.e. 4 meshes x 4 meshes), had 26 nodes and 50 components, and required a store of 33K using the more efficient GCAP2S program.

An alternative program, ECAP2S[165], and the larger facilities of the Midland Regional Computing Centre at Manchester, became available at a later date, but too late to be of use in this project. It is considered, however, that these facilities will adequately cope with the large circuit sizes, and may, therefore, be of interest for future research purposes.



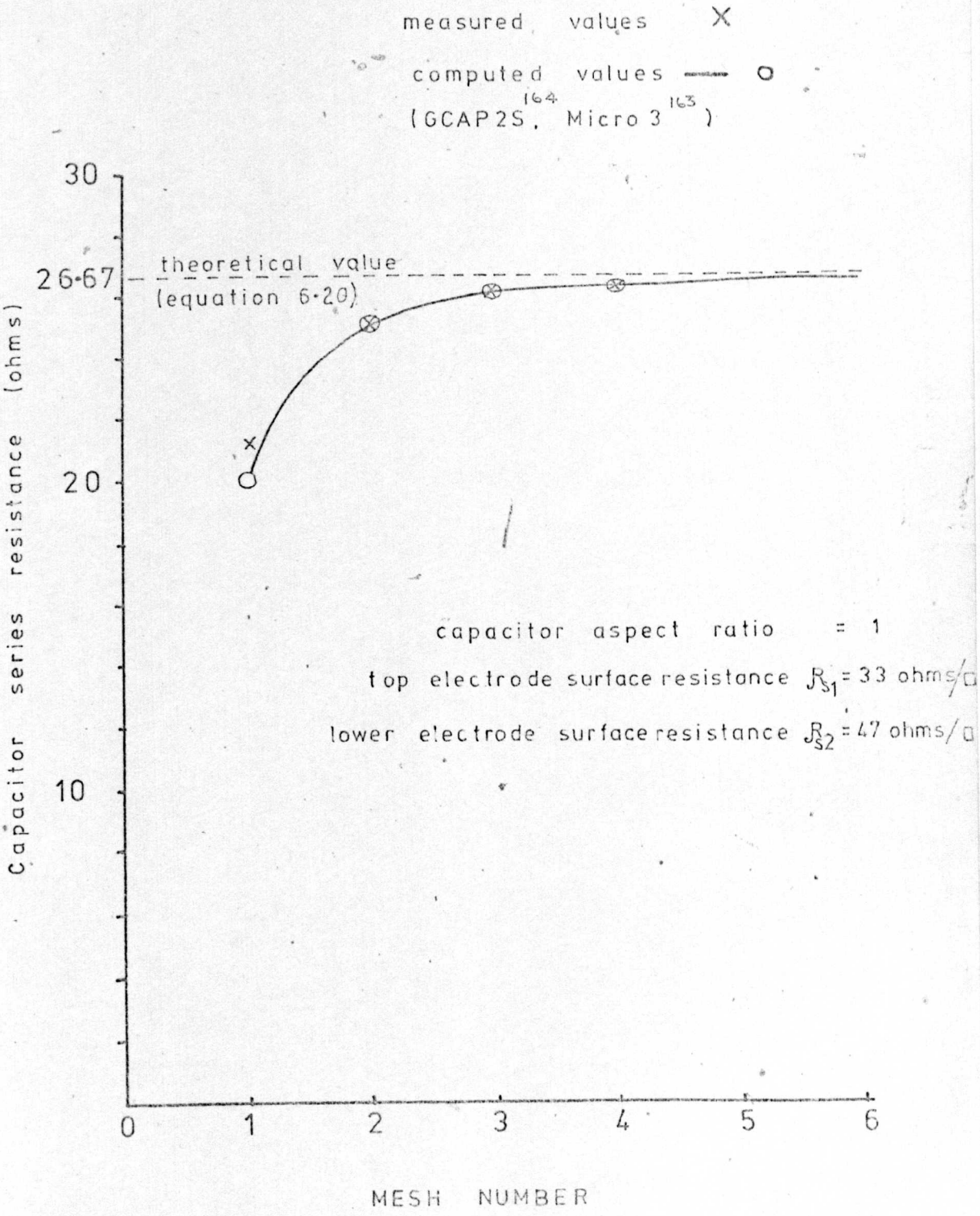


(b) actual model

Figure 6·16 2D 4mesh capacitor model (aspect ratio 1)

Figure 6·17

Capacitor electrode resistance as a function of the model mesh number



6.4.2 Results of the scaled model measurements.

The effect of the capacitor aspect ratio on the electrode Q factor.

Scaled models of a 1pF 3D configuration capacitor were constructed with a top electrode surface resistance of 0.033Ω/□ at 10 GHz, and a lower electrode surface resistance of 0.047Ω/□ , and the input impedance was measured, for selected values of capacitor aspect ratio (i.e. width/length). Graphs of the electrode series resistance and the Q factor, as functions of the capacitor aspect ratio, were then plotted, and are given in figure 6.18. Also shown in this figure, for comparison purposes, are the corresponding values for the 2D capacitor configuration, and in addition, values for the 3D capacitor, derived from an empirical expression, which will be referred to at a later stage in this Chapter.

From figure 6.18, it can be seen that the 3D configuration can lead to significant increases in the Q factor when compared to the 2D configuration (e.g. for an aspect ratio of 1, the increase in Q factor is approximately 75%).

The Q factor improvement is more significant for lower aspect ratio capacitors since (figure 6.19), withdrawing the current from the additional two edges of the lower electrode, has more effect on the total current distribution for low aspect ratio capacitors than it does for high aspect ratio capacitors.

The effect of the electrode resistivity on the electrode Q factor.

For capacitors with aspect ratios of unity, the electrode Q factor was measured as a function of

1) the top electrode surface resistance, as the lower electrode surface resistance is varied.
2) the lower electrode surface resistance, as the top electrode surface resistance is varied.

Graphs for both of these cases are shown in figures 6.20 and 6.21 respectively.

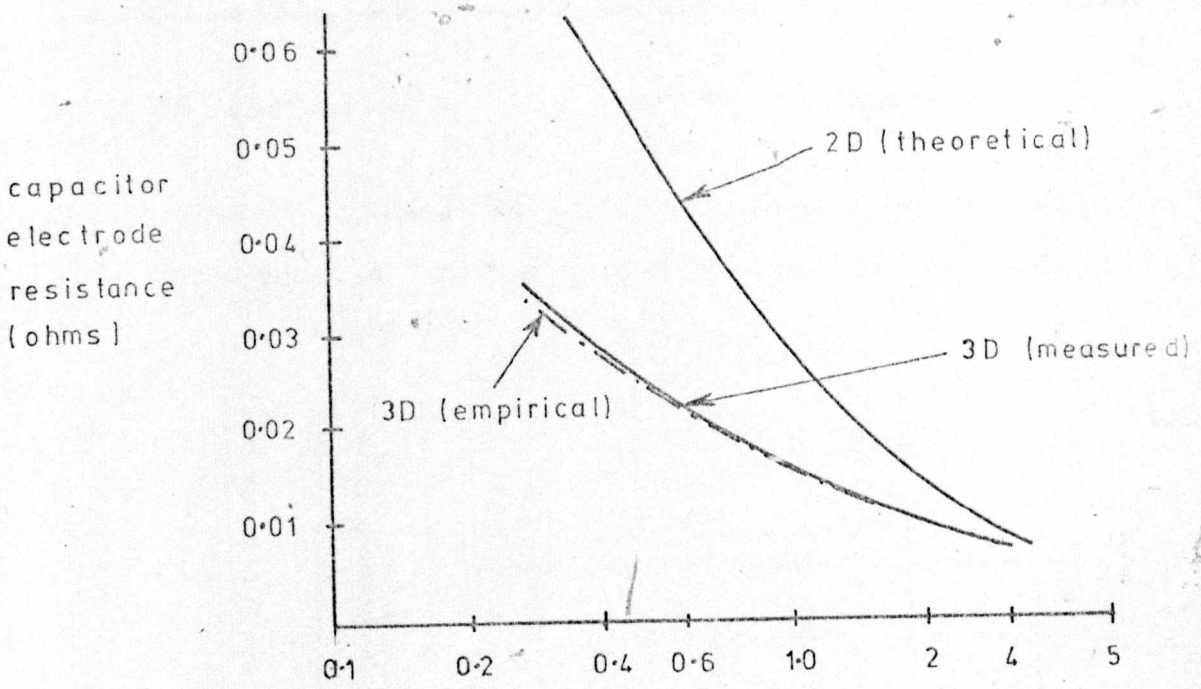
Figure 6·18

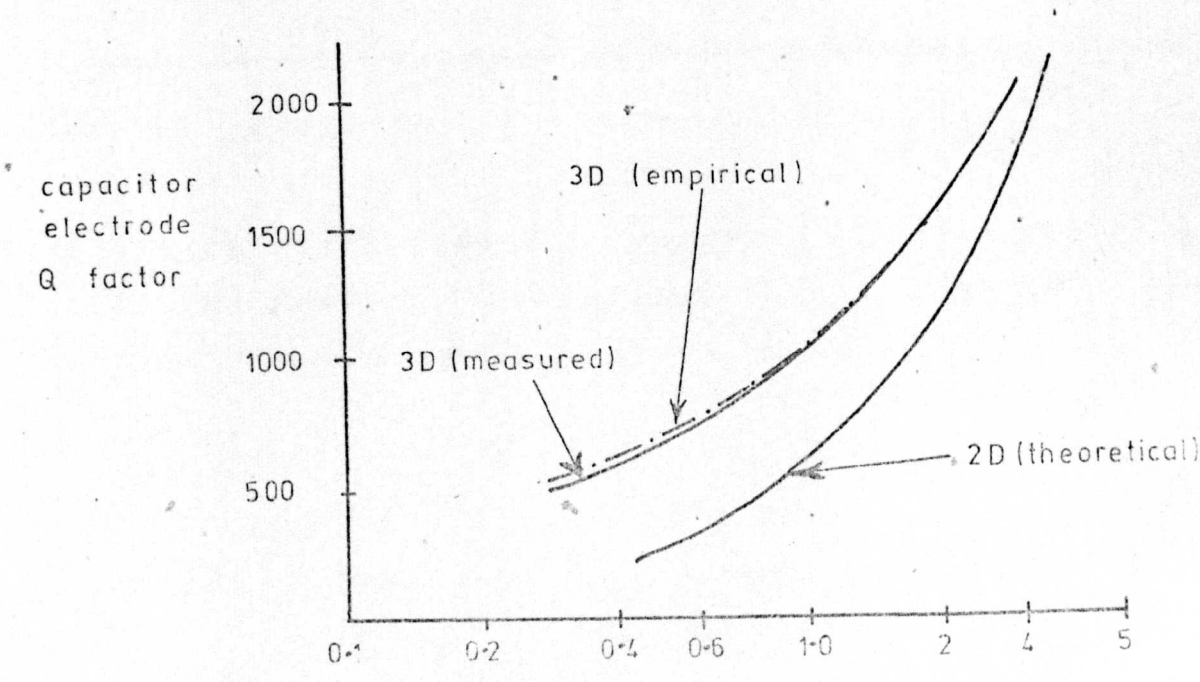
Capacitor electrode resistance and Q factor as a function of the capacitor aspect ratio.

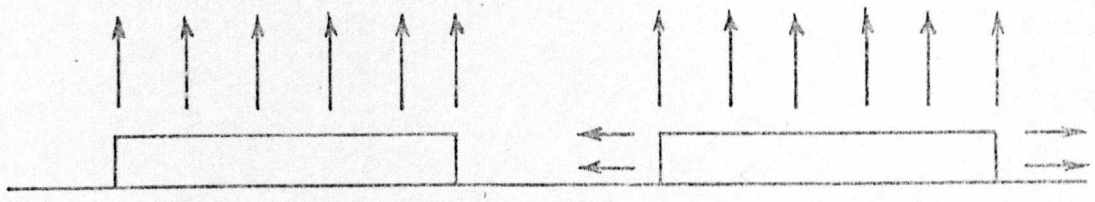
capacitance = 1 pF frequency = 10 GHz

top electrode surface resistance = 0·033 ohms/□

lower electrode surface resistance = 0·047 ohms/□

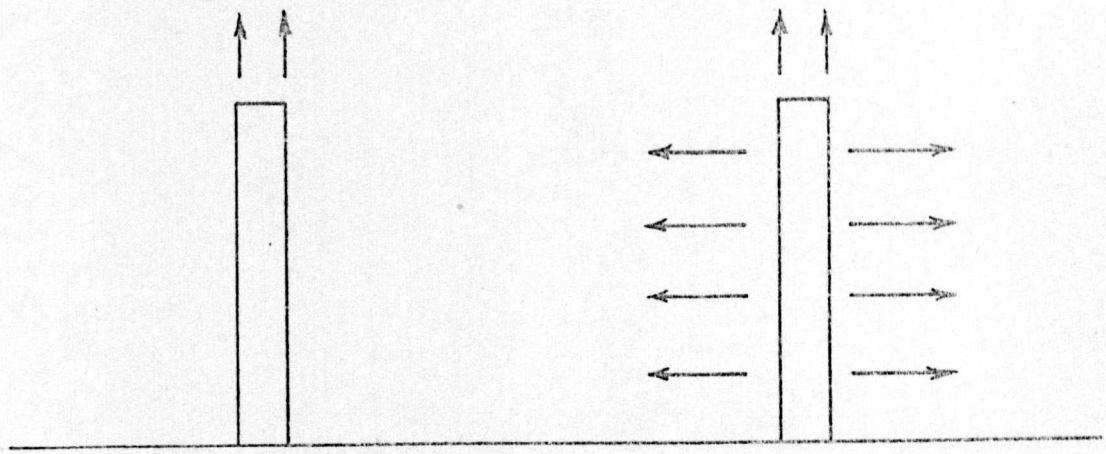






(a) 2D configuration (b) 3D configuration

A) LARGE ASPECT RATIO - resistance of the 3D configuration is comparable to that of the 2D configuration.



(c) 2D configuration (d) 3D configuration

B) LOW ASPECT RATIO - resistance of the 3D configuration is very much lower than that of the 2D configuration.

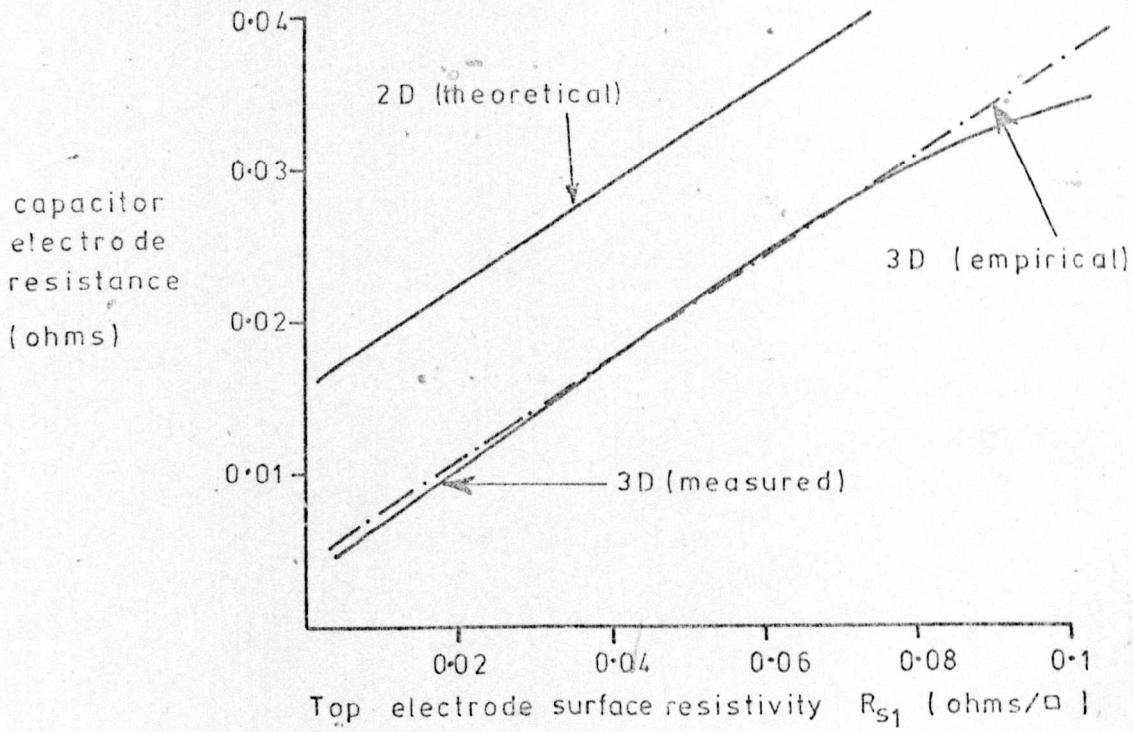
Figure 6-19 Plan view of the lower electrode of the 2D and 3D capacitor configurations showing the current flow as a function of the aspect ratio.

Figure 6·20

Capacitor electrode resistance and Q factor as a function of the top electrode surface resistance.

capacitance = 1 pF frequency = 10 GHz aspect ratio = 1

lower electrode surface resistance = 0·047 ohms/□



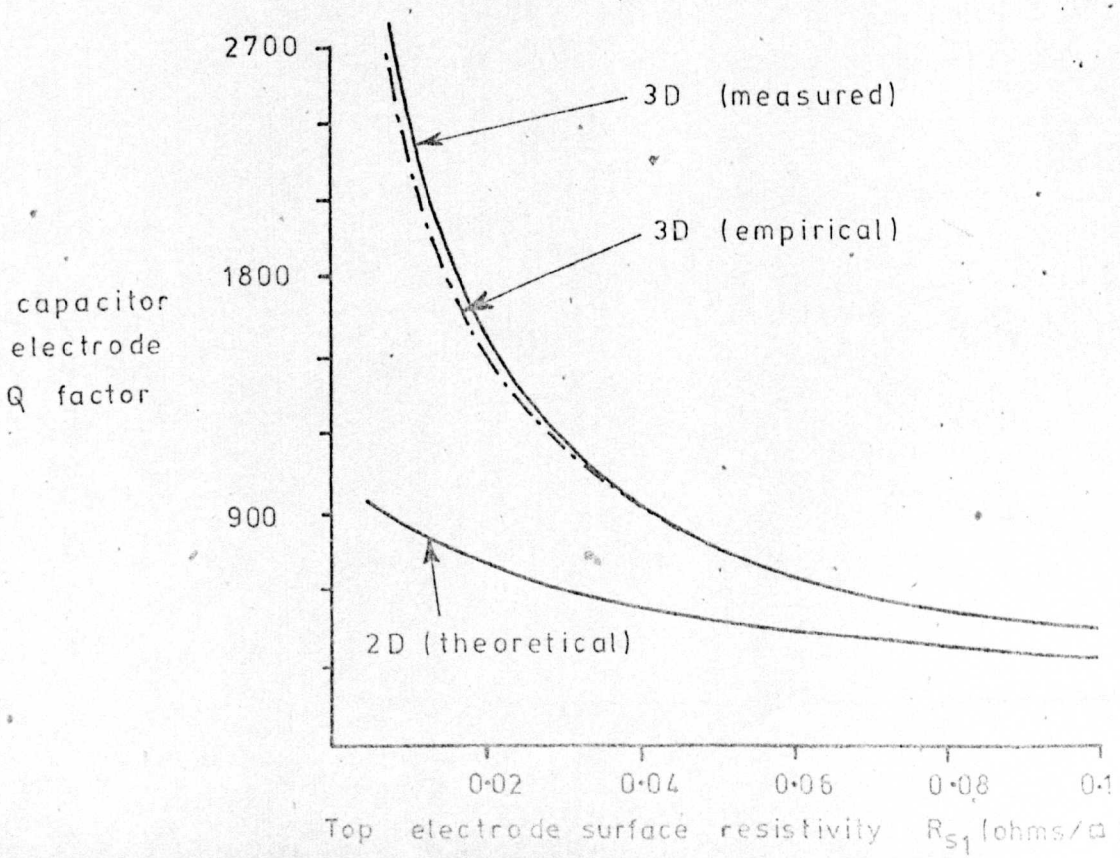
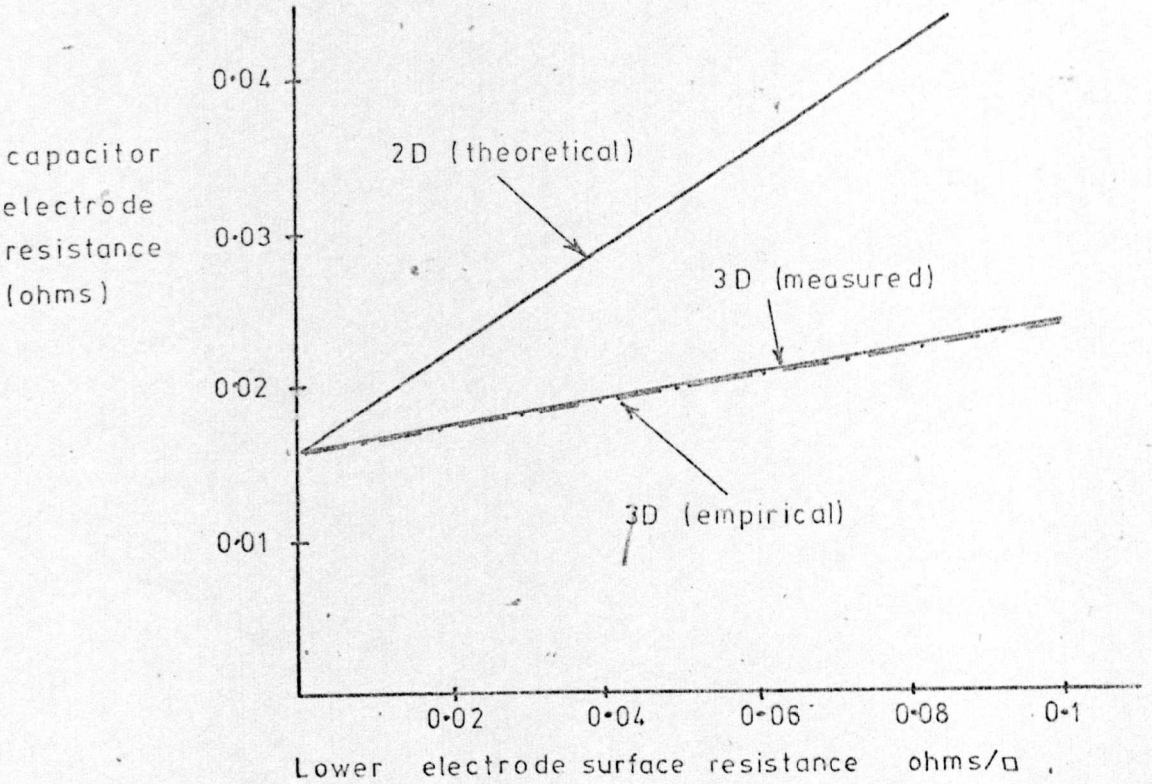


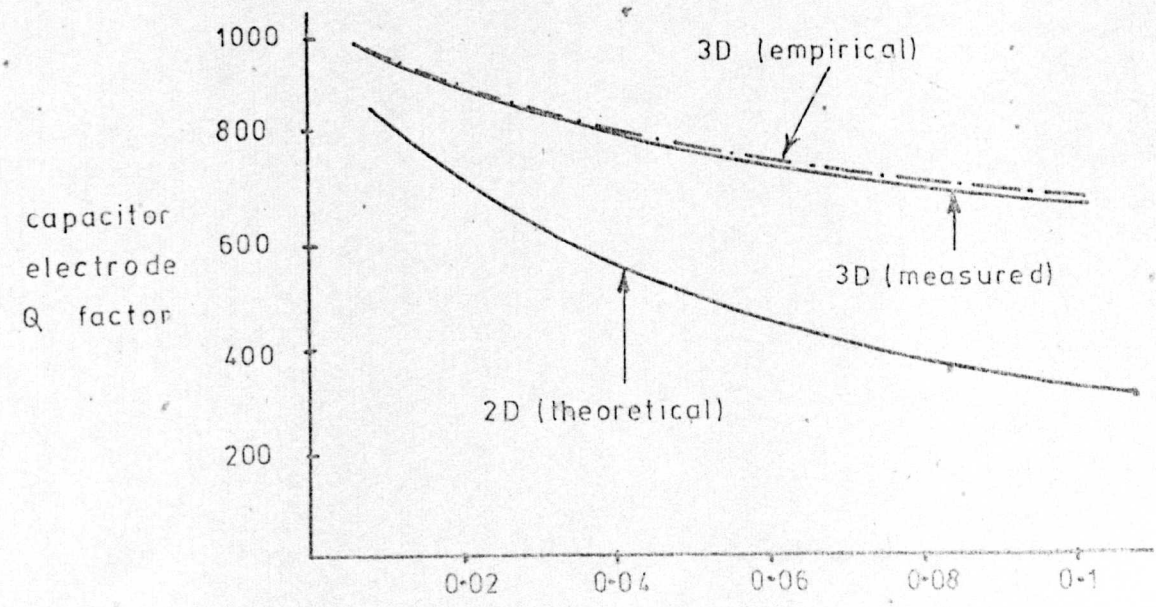
Figure 6·21

Capacitor electrode resistance and Q factor as a function of the lower electrode surface resistance.

capacitance = 1 pF frequency = 10 GHz aspect ratio = 1

top electrode surface resistance = 0·047 ohms/□





It will be observed that

1) for a given increase in the top plate surface resistivity, the increase in total electrode resistance is virtually identical for both the 2D and 3D configurations.
2) for a given increase in the lower electrode surface resistivity, the increase in the total electrode resistance is considerably less for the 3D configuration, than it is for the 2D configuration. This factor indicates that there is relatively little to be gained, for the 3D configuration, by increasing the thickness of the lower electrode to decrease the surface resistivity.

Empirical expression for the electrode resistance.

From the data displayed above for the 3D capacitor configuration, an empirical formula has been derived by the author, which relates the capacitor series resistance, R_c, to the top and bottom electrode surface resistivities, R_1 and R_2, and the capacitor aspect ratio, w/l_3. This empirical relationship is

$$R_c = \frac{1}{3}\left(\frac{w}{l_3}\right)^{0.4}\left(R_1 + 0.265R_2\right)\frac{l_3}{w} \qquad 0.1 \leq \frac{w}{l_3} \leq 5 \qquad 6.40$$

As was indicated previously, values obtained using this empirical expression have been compared with the measured values in graphs 6.18 - 6.21, and agreement between the measured and the empirical values, is in general, within 5%. This expression is used in the sections to follow, to characterise the electrode resistance of the 3D capacitor configuration.

6.4.3 Design summary for the 3D capacitor configuration.

It has been shown that for capacitors with aspect ratios less than 5, a considerable decrease in the electrode resistance can be achieved if the 3D configuration of figure 6.14 is used in preference to the 2D configuration of figure

6.6. For example, for a 1pF capacitor, with an aspect ratio of unity, the electrode resistance of the 3D capacitor is 75% lower than for the corresponding 2D capacitor.

It is assumed that a corresponding reduction in the electrode inductance will also be achieved.

For capacitors with aspect ratios in excess of 5, the properties of the 2D and 3D configurations are, to all intents and purposes, identical, and therefore the 3D configuration will not increase the upper practical limit of capacitance.

The 3D configuration is extremely useful, however, for low aspect ratio capacitors, as it significantly reduces the undesirable effects of the lower electrodes, and for this reason, the 3D configuration was used for the capacitors measured using the resonator measurement technique described in Chapter 5.

6.5 Impedance of the capacitor configuration used in the microwave measurement technique.

In the past, it has been impossible to reliably measure the properties of overlay capacitors, due to the parasitics introduced by the bond wires connecting the capacitor to the measurement system.

Introduction of the measurement technique described in Chapter 5, in which the bond wires have been eliminated, has permitted a much more accurate measurement of the capacitor properties, due to the substantial reduction in these parasitic effects.

To evaluate the characteristics of the capacitor dielectric materials themselves, from these measured capacitor properties, the small remaining parasitic effects must be determined. The rigorous determination of these parasitics is extremely difficult due to the complex physical arrangement of the capacitor in its measurement environment, and for the purposes of this investigation, an approximate solution is used, in which only the more significant of the parasitic effects are considered.

Errors introduced in the calculated dielectric properties as a result of the non-rigorous analysis, are

estimated to be less than 1%, as the parasitics themselves, have been reduced to an absolute minimum by the careful design of the capacitor and the test resonator (e.g. use of the 3D configuration to reduce the parasitic effects of the lower electrode, microstrip feeder lengths reduced to an absolute minimum, the use of copper as the electrode material, and a careful choice of the electrode thicknesses).

As the capacitor properties are determined from two microwave measurements, (i.e. before and after insertion of the test capacitor in the resonator), at two different measurement frequencies, it is essential to establish the parasitics present for each measurement, and to determine any changes in their characteristics which are encountered as a result of the change in frequency between the measurements.

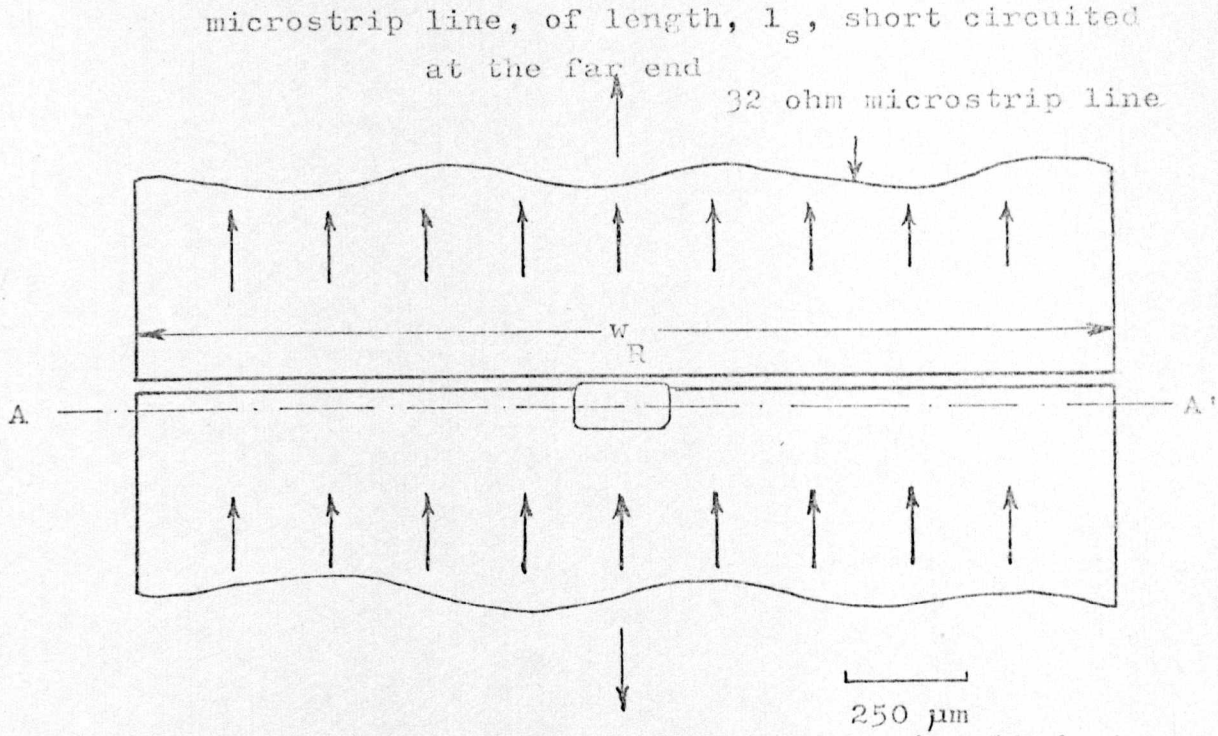
For the first microwave measurement (figure 6.23.a), in which the resonator characteristics are determined, the capacitor lower electrode and dielectric are already in position (Chapter 7), and the current distribution in the microstrip line is assumed to be constant as a function of the line width.

The lower electrode thickness is approximately 1 skin depth, and since the majority of current in the resonator is concentrated within 1 skin depth of the lower face of the microstrip line, (figure 6.23.b), the presence of the capacitor dielectric, and the reduction in the thickness of the microstrip conductor at this point, have negligible effect on the resonator properties. The capacitor lower electrode can then be assumed to be an inherent part of the resonant line, and its characteristics can therefore be included with the resonator characteristics.

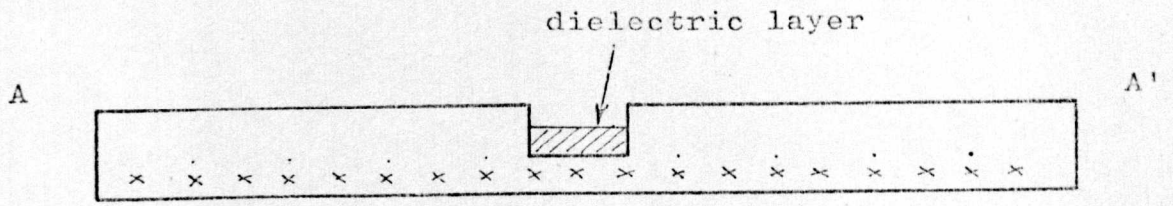
Conversely, virtually no current will flow through the capacitor dielectric, and it can be ignored in the equivalent circuit.

The equivalent circuit for the resonator for the first microwave measurement is then shown in figure 6.23.c, in which, C_g, is the gap capacitance.

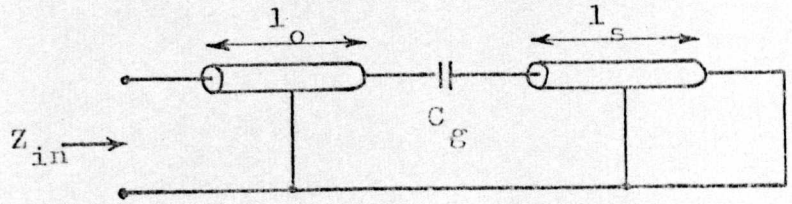
For the second measurement (figure 6.24.a), the top electrode of the capacitor is connected in position, and this results in the following modifications to the equivalent



a) Schematic diagram of the capacitor and the resonator.



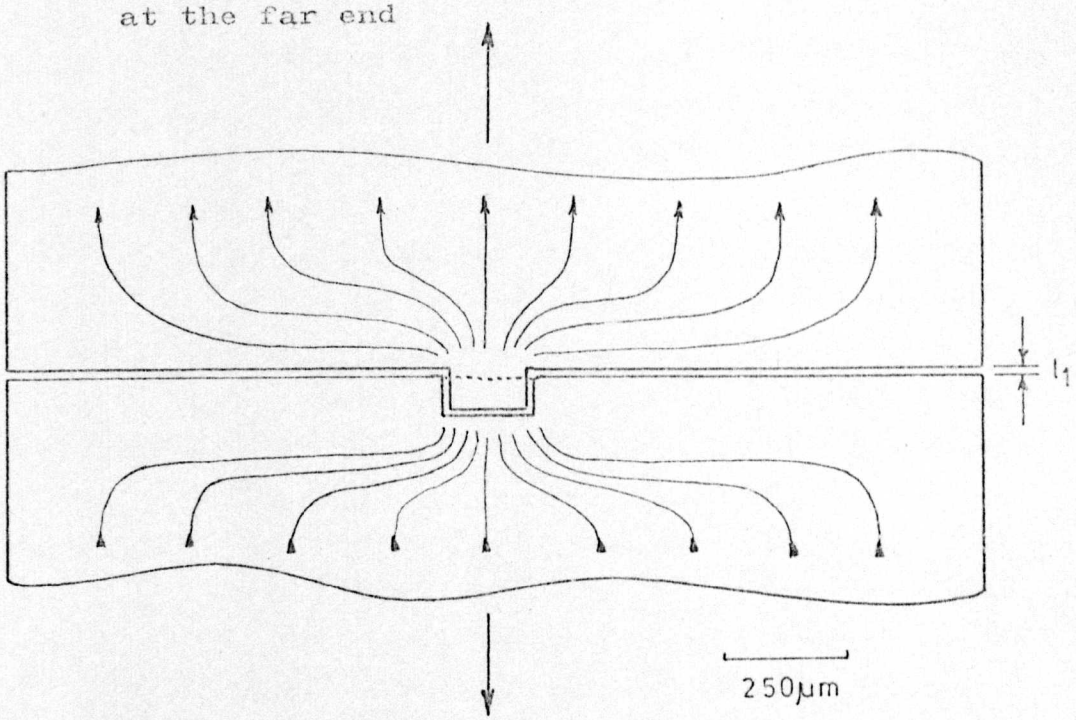
b) Cross-section on AA', showing uniform current distribution as a function of line width, and non uniform current distribution as a function of thickness.



c) Equivalent circuit of capacitor and resonator.

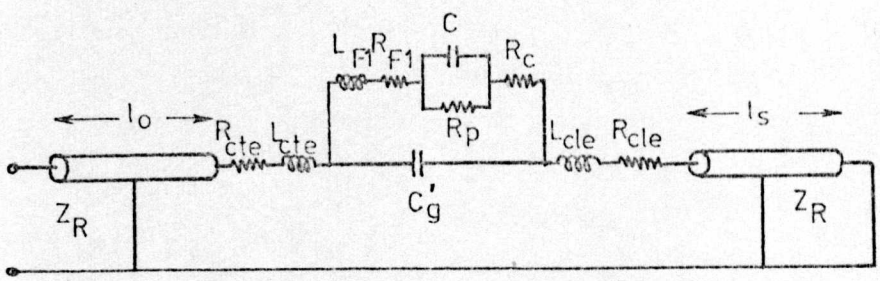
Figure 6.23 Configuration for the first microwave measurement.

microstrip line, of length, l_s, short circuited at the far end



microstrip line, of length, l_o, open circuited at the far end

a) Schematic diagram of the capacitor and a section of the resonator.



L_{cte}, R_{cte} current crowding impedance -- for microstrip line connected to the top electrode,

L_{cle}, R_{cle} current crowding impedance -- for microstrip line connected to the lower electrode,

L_{F1}, R_{F1} impedance of top electrode microstrip feeder,

R_c resistance of the capacitor electrodes,

C'_g modified gap capacitance,

b) Equivalent circuit of the capacitor and resonator.

Figure 6.24 Configuration for the second microwave measurement.

circuit;

1) as indicated in figure 6.24.a, the current distribution at the gap, as a function of the resonator width, will no longer be uniform due to the effective short circuit of the test capacitor.

The current crowding introduces additional resistance and inductance in series with the microstrip gap capacitance (R_{cte}, L_{cte}, R_{cle}, L_{cle} in figure 6.24.b.). Due to the differing current distributions on either side of the gap, the current crowding effects will not be identical.

To establish the magnitude of these current crowding effects, scaled models of the impedance steps (at 200 x full size), were constructed using Teledeltos paper (figure 6.25.a and b), and the current flow paths were plotted. From the resulting field diagrams, the effective width, w_E, of the microstrip line, in the proximity of the impedance step, was determined as a function of the distance, r, from the microstrip gap. The current distribution was observed to be uniform for distances greater, or equal to, 5w from the microstrip gap. For each of the impedance steps, the additional inductance and resistance, due to the current crowding, for microstrip lines of length, 5w, were then calculated using equations 6.11 and 6.8, in which numerical integration techniques were employed to take into consideration the variation of the effective line width.

The derived values of the current crowding resistors and inductors, for capacitor dimensions typical of those used in the microwave measurements, are summarised in figure 6.26. It will be observed that the resistor values are given in terms of the surface resistivity of the microstrip conductors, and it will be recalled from Appendix 1.3 that

$$\mathcal{R}'_{SI} = \alpha_c Z_R w_R \qquad 6.41$$

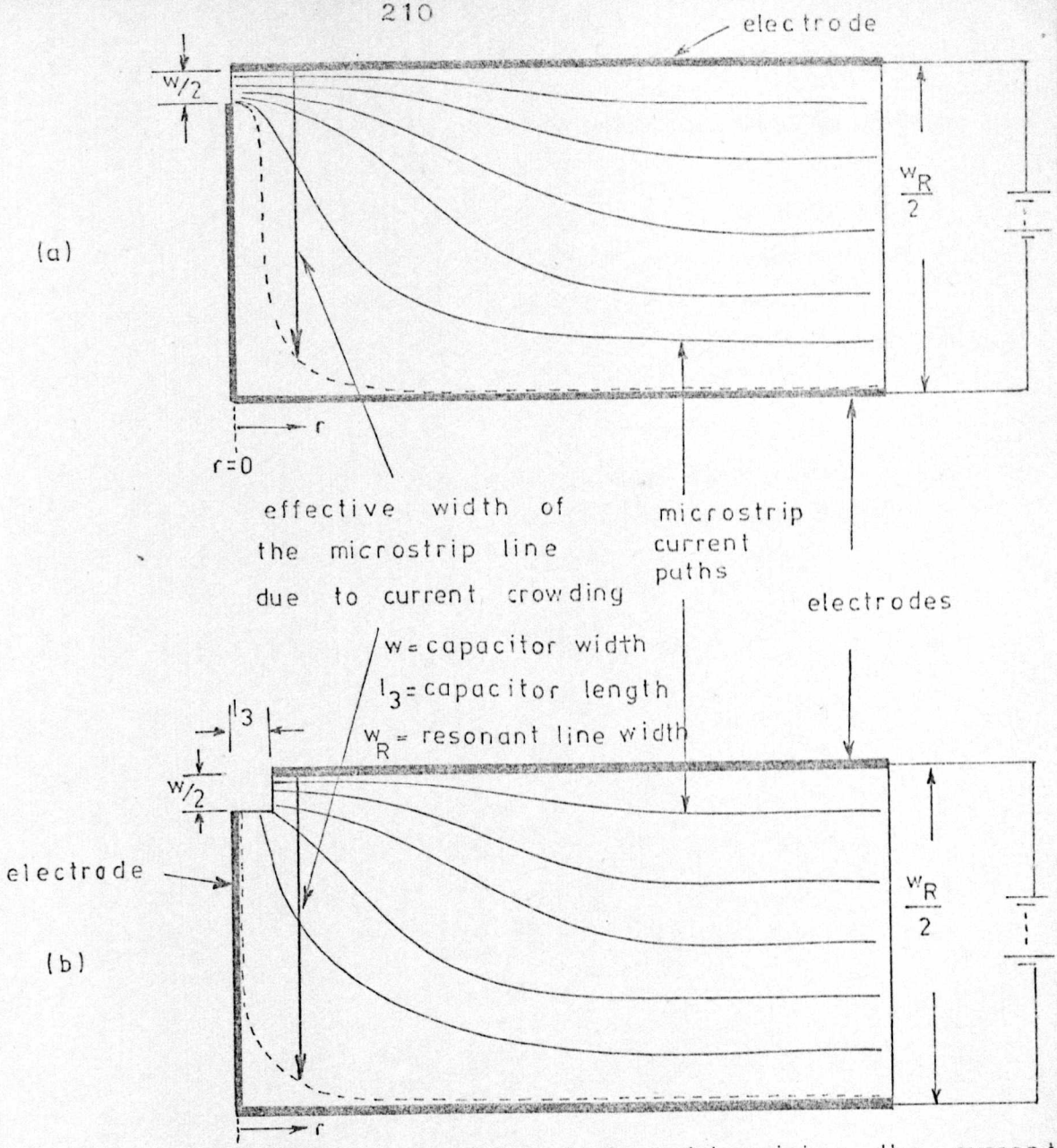


Figure 6·25 Experimental arrangement for determining the current flow paths in the microstrip lines connected to
a) the capacitor top electrode
b) the capacitor lower electrode

Current crowding resistance and inductance assuming $l_3 = w/2 = w_R/20$	RESISTANCE Ω	INDUCTANCE nH
R_{cte} , L_{cte} (figure 6·25.a)	$0{\cdot}0247\ \mathcal{R}'_{s1}$	0·031
R_{cle} , L_{cle} (figure 6.25.b)	$0{\cdot}0081\ \mathcal{R}'_{s1}$	0·0021

Figure 6·26 Current crowding parameters used in the equivalent circuit of figure 6·24

where R'_{s1} is the surface resistivity of the microstrip line,

α_c is the attenuation coefficient of the microstrip line (which is measured in the microwave measurements),

Z_R is the resonator characteristic impedance,

w_R is the resonator line width.

The additional resistance and inductance due to the current crowding effects, can therefore be readily calculated for each of the test resonators.

2) the gap capacitance, C_g, is reduced to

$$C'_g = \frac{w_R - w}{w_R} C_g \qquad 6.42$$

due to the removal of that part of the gap occupied by the top electrode. The resulting change in gap capacitance is 10%, which is approximately 1% of the test capacitance.

3) the resistance of the top electrode feeder, of length, l_1, is, from equation 6.12

$$R_{F1} = R'_{s1} \frac{l_1}{w} \qquad 6.43$$

where R'_{s1} is as defined in equation 6.12.

4) the inductance of the top electrode feeder is, from equation 6,13

$$L_{F1} = \frac{Z_F}{v} l_1 \quad H \qquad 6.44$$

where Z_F is as defined in equation 6.13.

5) the additional resistance introduced due to the top electrode of the capacitor is, from equation 6.40

$$R_c = \frac{1}{3}\left(\frac{w}{l_3}\right)^{0.4} R'_{si}\,\frac{l}{w}3 \qquad 6.45$$

6) from the preceding discussions on the electrode inductance (section 6.2.2) and the current crowding effects, it can be deduced that there is negligible additional inductance introduced by the capacitor electrodes themselves.

The equivalent circuit for the capacitor and resonator, for the second microwave measurement, is therefore as shown in figure 6.24.b, in which the capacitance, C, is defined by

$$C = \frac{e_o e_d\, w\, l_3}{t_3} \qquad 6.46$$

in which e_d is the dielectric constant
t_3 is the dielectric thickness.

The dielectric loss resistance is given by the shunt resistance, R_p.

Using this equivalent circuit, and the data already provided in Chapter 5 for the complete resonator equivalent circuit, an accurate evaluation of the microwave properties of the dielectric materials can be achieved.

6.6 Conclusions.

In this chapter, the properties of the most common microwave overlay capacitor configuration (i.e. the 2D configuration of figure 6.6), have been investigated in detail, and the analysis has shown that;

1) the lower electrode contributes more to the electrode loss than does the top electrode,

2) the effects of the input microstrip feeders can be significant, and they should be kept as short as possible,

3) the optimum top electrode thickness is 1.57 skin depths, and the optimum lower electrode thickness is 1 skin depth,

4) there are significant advantages to be gained by using a material with an extremely high conductivity for the lower electrode,

5) the capacitor aspect ratio is vitally important in determining the magnitude of the parasitic inductive and resistive effects,

6) for lumped element capacitors on quartz substrates at 10 GHz, using the 2D configuration, the practical upper limit of capacitance, using silicon dioxide dielectric, is 2.5pF, and using alumina dielectric, is 4pF, due to the parasitic inductance. Higher capacitance values can only be reliably achieved by using higher dielectric constant materials for the capacitor dielectric,

7) for capacitors with aspect ratios less than 5, a significant reduction in the parasitic effects can be achieved by using the 3D electrode configuration of figure 6.14.

In addition, an estimation has been made of the parasitics encountered during the measurements of the microwave properties of overlay capacitors, using the measurement technique described in Chapter 5, and this permits the determination of the dielectric loss and the dielectric constant from the measured capacitance and Q factor.

The complete measurement procedure to determine these properties, is given in the following chapter.

7. OVERLAY CAPACITOR PROCESSING TECHNIQUES.

7.1 Introduction.

In this chapter, a comprehensive processing guide to the fabrication of thin film overlay capacitors is presented. The particular processing techniques described were adopted to achieve the design recommendations outlined in the preceding chapter.

In addition, a method is described for the integration of overlay capacitors with the microstrip resonator used in the measurement technique of Chapter 5, as a guide for other researchers currently considering utilising the measurement system.

The processing techniques using gold technology, which are described in this chapter, were devised in collaboration with Mr. R.S.Butlin, a fellow research student.

7.2 Capacitor design requirements.

In addition to the design proposals of the preceding chapter, the following requirements have been considered in the fabrication process.

1) the dielectric area must be defined (figure 6.6.a). A blanket layer of dielectric covering the whole substrate area is not acceptable in the majority of applications.

2) from figure 6.6.b, it can be seen that the dielectric is in contact with both the lower electrode and the substrate. The contact with the substrate is essential to prevent a short circuit between the electrodes when the top electrode is connected. This introduces problems when the capacitor dielectric and the substrate are of the same, or similar, materials, as etching of the dielectric will result in etching of the substrate.

It is also essential that the dielectric layer should be free from voids and pinholes to prevent short circuits forming when the top electrode is connected, and to prevent low voltage breakdown.

3) it has been shown by Tolliver[166] from studies of silane-deposited silicon dioxide over metal contours, that a predominant factor in determining the final oxide contour over an etched metal step, is the thickness of the metal, and a second, closely interrelated, factor is the degree of bevel, or undercutting, obtained during the metal etch. To facilitate the dielectric overlapping the electrode step, the lower electrode should be relatively thin, and the edge profile tapered as shown in figure 6.6.b. Similar requirements can be deduced for the dielectric layer, where the top electrode overlaps the dielectric.

4) to reduce the capacitor electrode losses, the electrode materials must have a high conductivity and a low surface roughness. Due to the multi-layer nature of the component, this necessitates that all three layers must have a low surface roughness. This feature is essential, in particular, for the lower electrode, to avoid low voltage breakdown of the capacitor.

7.3 Basic features of the processing techniques.

The most important features of the overlay capacitor fabrication process, which is descibed in Appendix 7.1, are

1) copper electrodes are used due to their high conductivity. Processing techniques for gold electrodes are also described, however, as there tends to be fewer processing difficulties with the gold technology.

2) a tapered lower electrode edge profile was obtained by dip-etching techniques, using ferric chloride as an etchant (assuming copper electrodes), as this technique produces more undercutting (i.e. more taper) than other etching techniques (section 2.4.10). This then produced a lower electrode step which could easily be completely coated by the dielectric (figure 7.1), reducing the possibility of low voltage breakdown, or pinholes at the step.

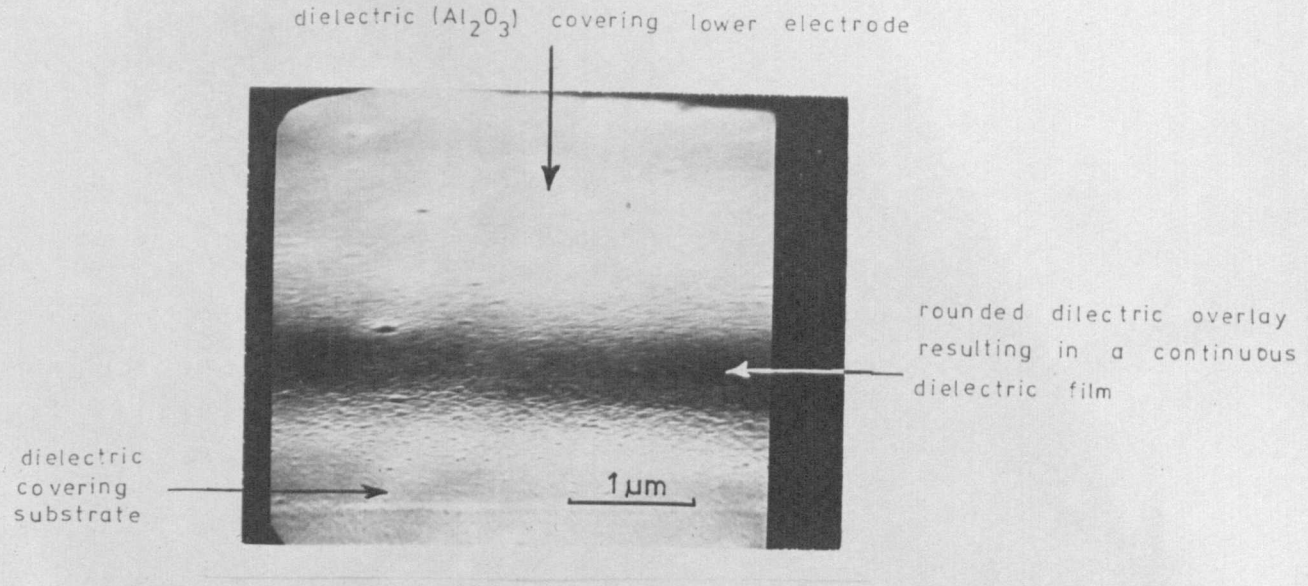


Figure 7-1 Dielectric film completely covering a tapered lower electrode step.

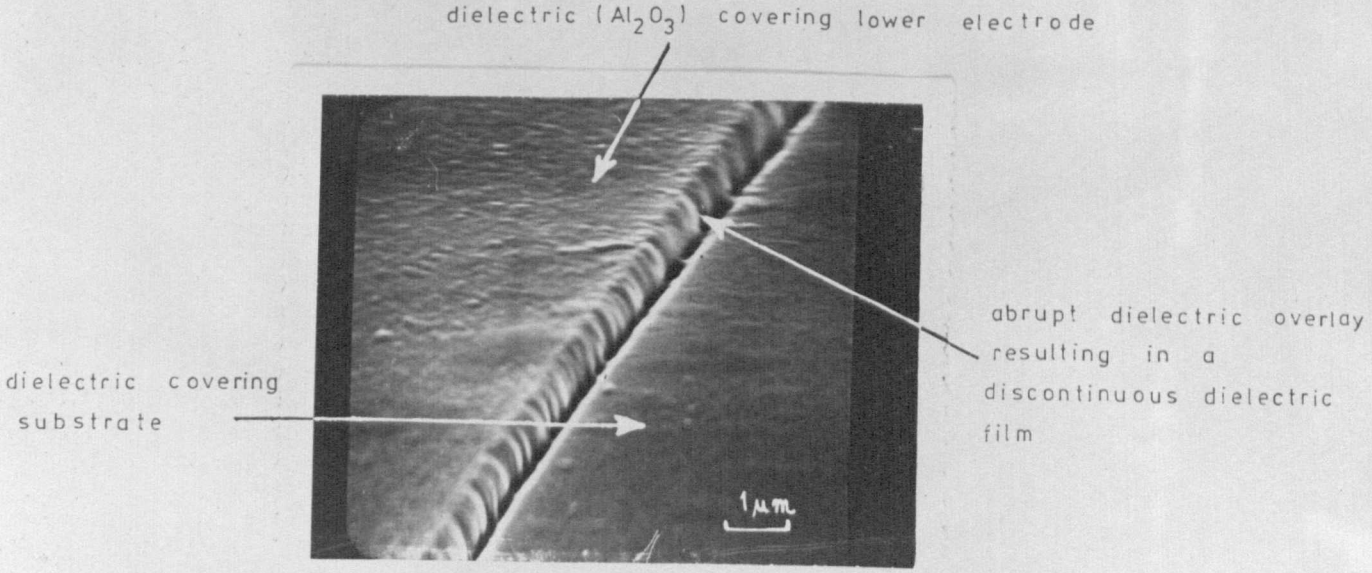


Figure 7-2 Discontinuity in dielectric film covering an abrupt lower electrode step.

Normal "jet" etching techniques, as used in the remainder of the process, result in an abrupt lower electrode step (figure 7.2), which does not allow adequate coverage when the dielectric is deposited.

3) the dielectric layer is deposited by r.f. sputtering techniques. The dielectric area is defined using a new photolithographical method[167] developed specifically for this application, which eliminates etching of the dielectric, as this would result in etching of the substrate (section 7.2).

Additional advantages of this technique, which is described in detail in Chapter 12 (section 2), are

a) the formation of pinholes in the dielectric layer, due to the presence of dust particles during the photolithographical stages (i.e. mask production, photoresist application, exposure and development), is eliminated due to a metal masking layer below the photoresist negative relief mask[168, 169].

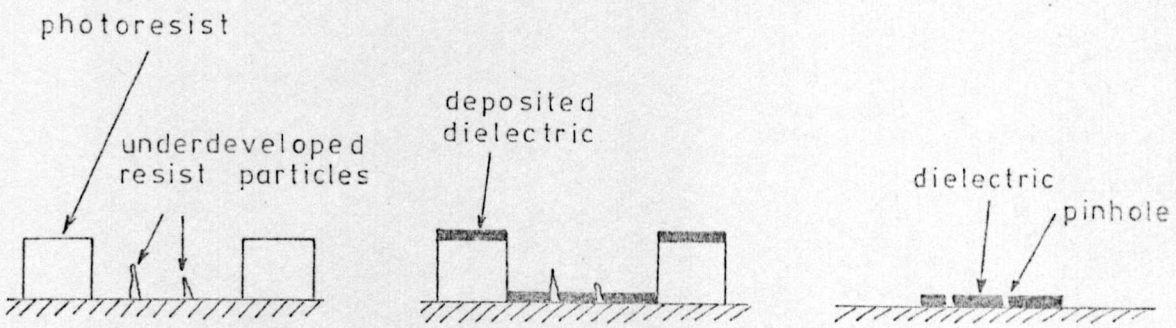
Dust particles produce areas of underexposed and underdeveloped resist, which, in this technique, are removed when the metal layer itself is removed prior to dielectric deposition (figure 7.3).

b) the dielectric edge profile can be tailored to the desired taper (figures 7.4 and 7.5) by careful selection of the metal protective layer thickness with respect to the dielectric thickness, and the etching time for the masking layer, as described in Appendix 7.2 (note 3).

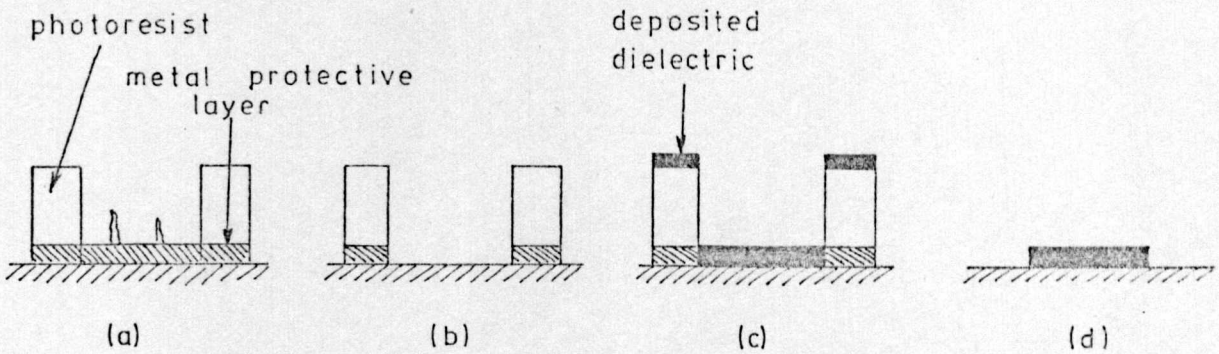
c) etching of the dielectric is avoided, and thus many of the difficulties associated with the use of the extremely active etchants are also avoided.
e.g. inadequate masking of the circuit, handling of hydrofluoric acid.

d) the resolution of the deposited dielectric is considerably better than can be achieved by out-of-contact masking techniques[170].

e) the metal protective layer protects the complete circuit during the majority of the processing. It therefore improves the adhesion of subsequent



A). Conventional photoresist negative-relief-mask technology (producing a film with pinholes)



B) Composite negative-relief-mask technology (producing a pinhole-free film)

Figure 7·3 Negative-relief-mask techniques

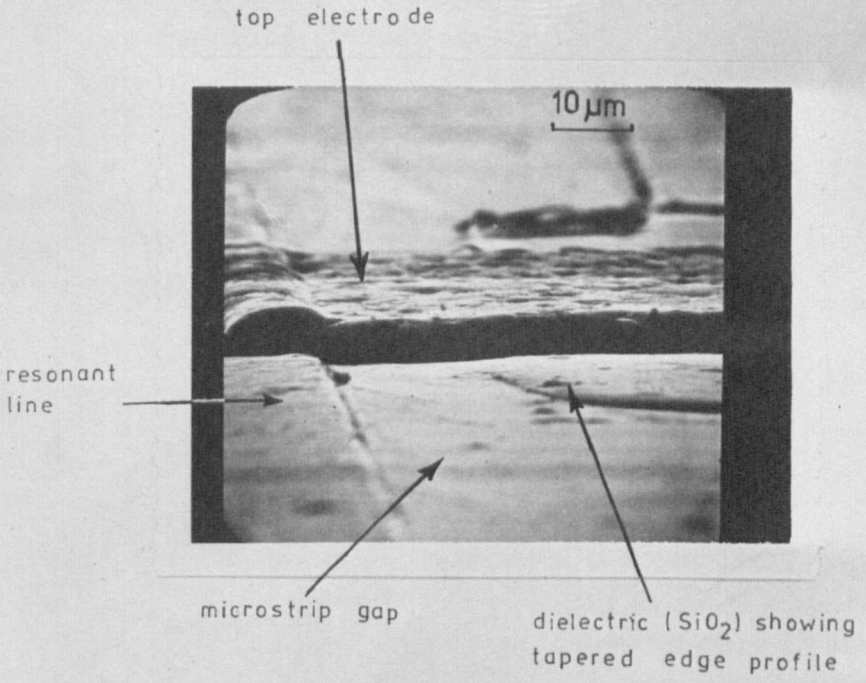


Figure 7·4 Tapered edge profile of dielectric

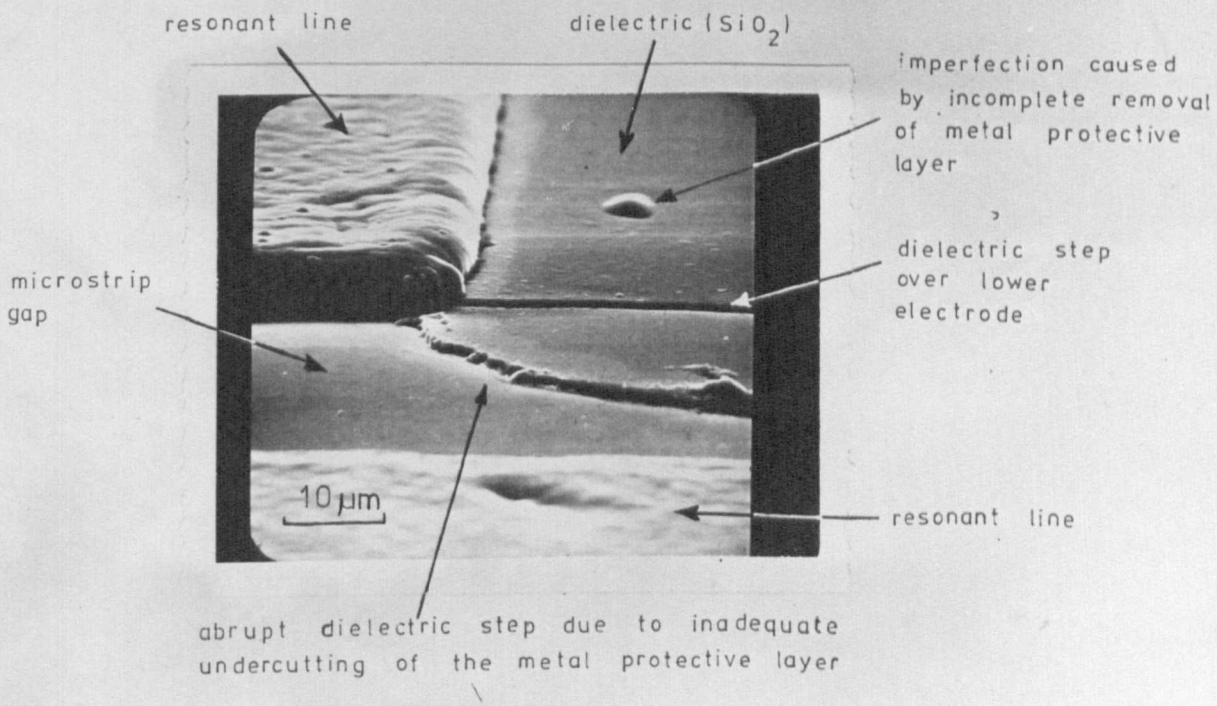


Figure 7·5 Abrupt edge profile of dielectric

deposited layers, including the dielectric, as these layers are deposited onto surfaces which have not been exposed to photoresist[171]. The metal layer also improves the definition at subsequent etching stages as it acts as an in-contact metal mask below the photoresist mask (figure 7.3), which reduces undercutting.

7.4 Measurement system restrictions.

The measurement technique for the evaluation of the microwave properties of overlay capacitors, involves the comparison of the return loss (Q factor) and resonant frequency of a microstrip resonator before and after the test capacitor is inserted. It was initially considered a practical proposition to construct one standard resonant line, to measure the return loss and resonant frequency, and then to compare these with the corresponding parameters for other "identical" lines, but with test capacitors inserted. The difference in the measured properties would then be due to the capacitor characteristics. However, preliminary measurements showed that this approach would considerably limit the overall measurement technique accuracy due to the large spread in microstrip resonator Q factors (typically 12%) for nominally identical lines, due to processing variations.

The reference-line technique was therefore discarded, and resort made to measuring each individual line before and after insertion of the test capacitor. This approach results in a higher overall measurement accuracy as the repeatability of return loss and resonant frequency measurements for individual lines is considerably better than repeatability in the processing of nominally identical lines. This technique does, however, introduce the problem of integration of the capacitor with the resonant line so that the microwave measurements can be performed both before and after insertion of the test capacitor, and so that the original line characteristics are not affected by the additional processing stages which the line must be subjected to when the test capacitor is inserted.

Integration of the capacitor with the resonant line.

In Chapter 6, the 3D capacitor configuration (figure 6.14) was shown to have a higher Q factor than the 2D configuration, and on this basis it was decided to limit initial investigation to the 3D configuration.

The location of the capacitor in the resonator is shown in figure 7.6.a, and the construction of the capacitor, as an integral part of the resonator is shown in figures 7.6.b and 7.6.c.

The processing and measurement sequence consists of performing the initial microwave measurement of the line properties with the lower electrode and dielectric already in position (figure 7.7.a). The second measurement is then made with the top electrode in position (figure 7.7.b). Compared with other techniques, this approach reduces the processing stages between the measurements, brings the process stage with the lowest yield (i.e. the dielectric deposition stage) before the time consuming electrical measurements, and overall, reduces the total number of processing stages.

The only difference between the capacitors used in this measurement technique and those used in normal applications, is that in the latter, the top electrode and lower electrode feeder are electroplated at the same processing stage, whereas in the former, the top electrode is deposited, defined and electroplated after the lower electrode feeder is plated. The requirements of the measurement technique therefore introduce more processing stages, but fundamentally do not change the basic capacitor configuration or properties.

An additional restriction imposed by the measurement technique is that the leading edge of the capacitor dielectric layer must fall within the microstrip gap (figure 7.6.b). As the resist thickness used in the deposition of the dielectric is of the order of 15 μm, and the microstrip gap is approximately 25 μm in width, a reasonable degree of dimensional control is necessary at the photoresist stage to obtain high processing yields. In normal capacitor design, it is unlikely that such a requirement would be necessary.

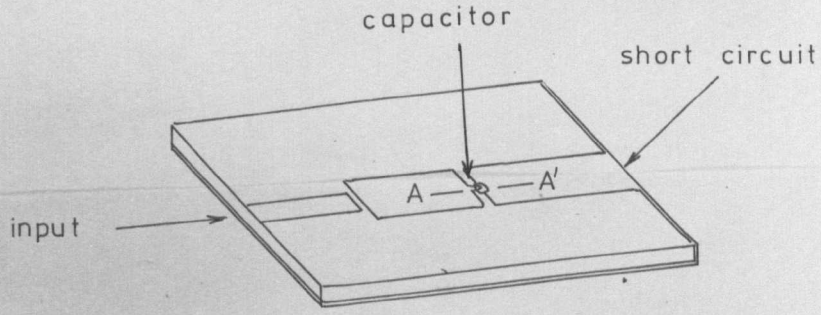


Figure 7·6 (a) Position of the capacitor in the resonator

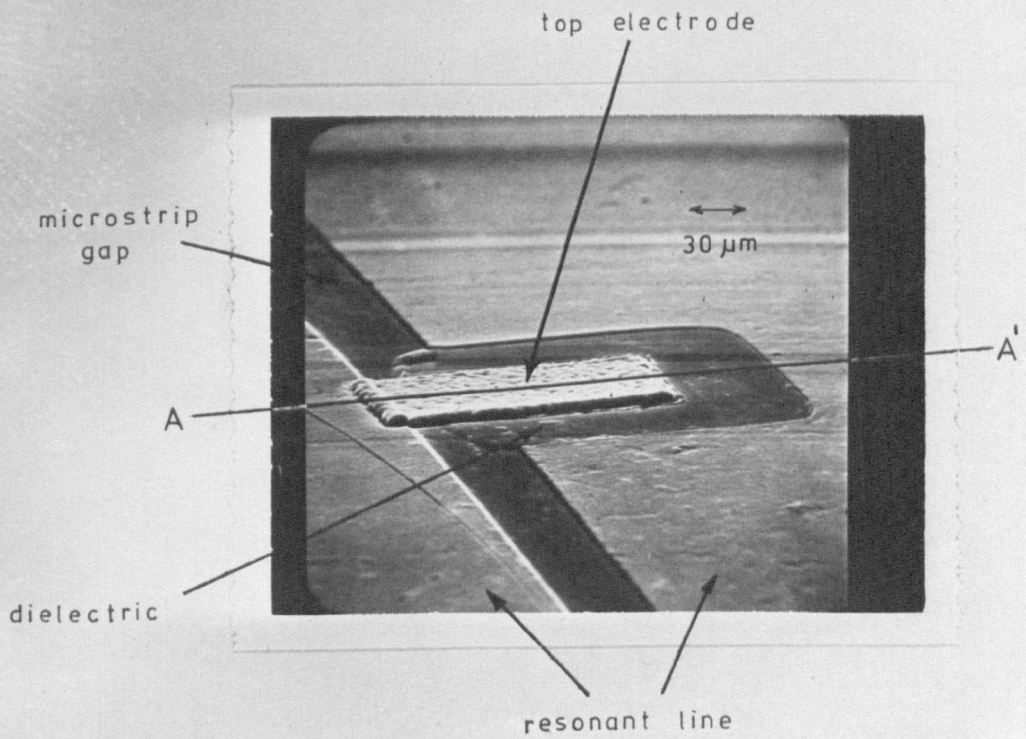


Figure 7·6 (b) Integration of capacitor and resonant line.

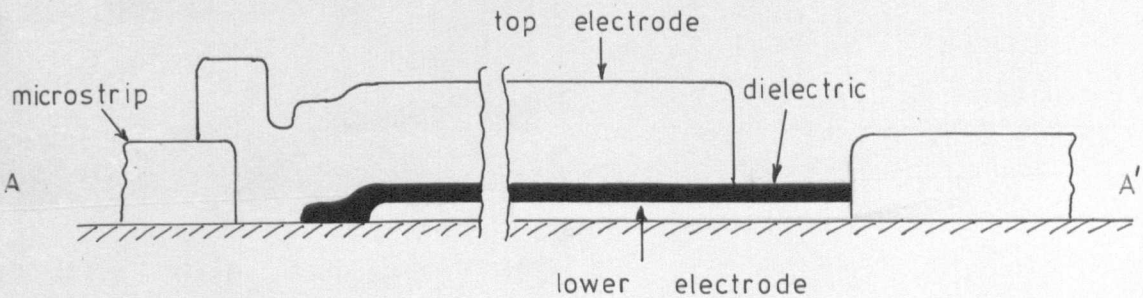
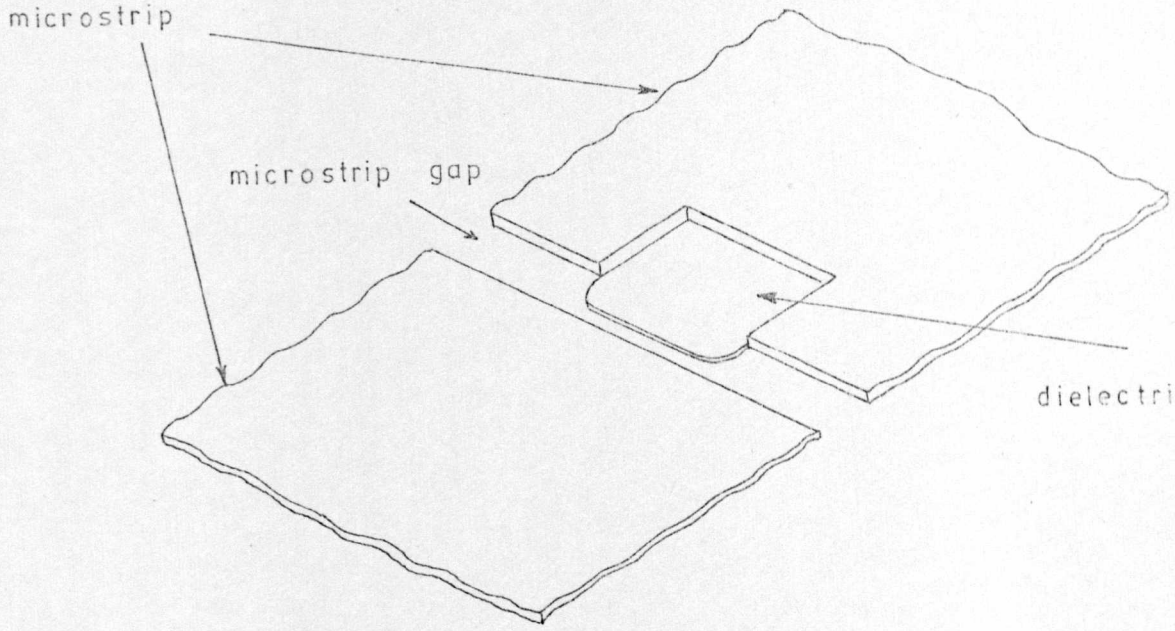
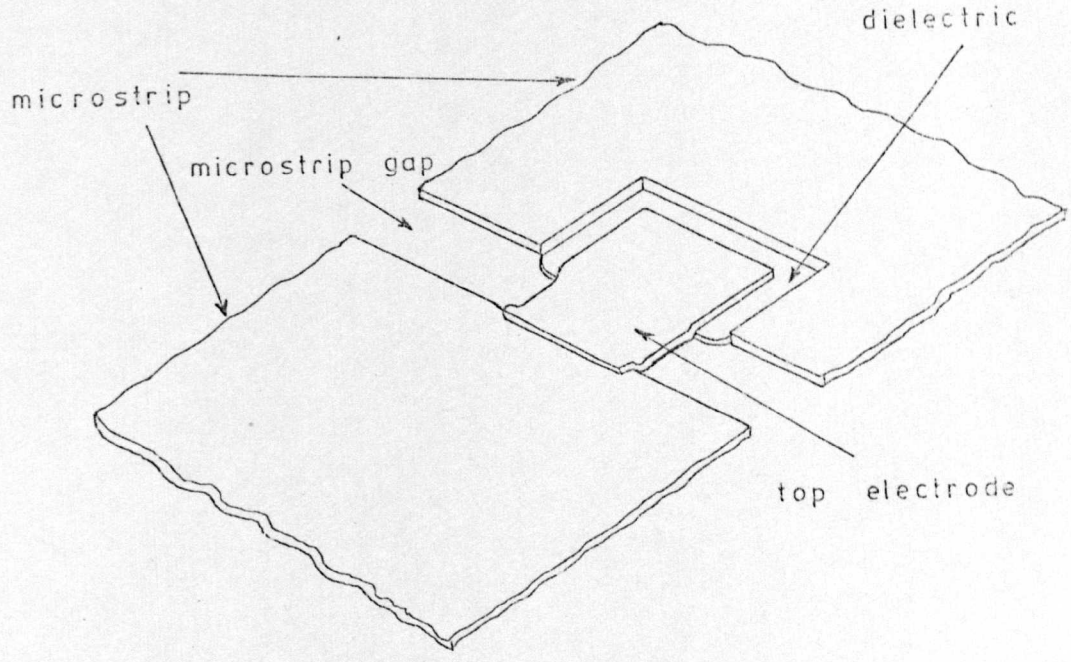


Figure 7·6 (c) Cross-section of capacitor

Figure 7·6 Integration of test capacitor and resonator



(a) Without top electrode



(b) With top electrode

Figure 7-7 Capacitor state at (a) first measurement (b) second measurement

7.5 Overlay capacitor processing procedure.

The preceding sections have outlined the most important features of the processing techniques for the fabrication of thin film overlay capacitors, and a detailed step-by-step account of the complete processing procedure is given in Appendix 7.1.

7.6 Processing observations.

7.6.1 Formation of pinholes.

In the initial stages of capacitor fabrication, using silicon dioxide as dielectric, yields were non-existent due to high pinhole counts.

On introduction of the composite negative-relief-mask technique, the pinhole count was decreased to a tolerable level so that silicon-dioxide capacitors could be produced, albeit with a yield of approximately 20%. This emphasises the tremendous importance of avoiding circuit contamination during the processing, and it is evident that a much higher degree of clean-room-control is required for overlay capacitor manufacture than for other thin film components. Every precaution should therefore be taken to avoid contamination by the environment, and all chemicals should be filtered prior to use.

On the basis of these factors, it was realised that during, and after, the removal of the metal protective layer of the negative-relief-mask, the devices are extremely susceptible to contamination, which would directly result in pinhole formation in the dielectric. Therefore, additional precautions to reduce possible contamination, described in Appendix 7.2, were instigated, which immediately improved the circuit yield to approximately 75% for silicon dioxide capacitors.

The initial design of the capacitors required dielectric thicknesses of approximately 1 μm, and lower electrode thicknesses of approximately 0.75 μm, and it became immediately obvious from s.e.m. studies of these capacitors, of the importance of the profile of the lower

electrode if an acceptable dielectric is to be achieved, confirming the observations of Tolliver[166].

Initial profiles, obtained by "jet" etching techniques using the sulphate etchant (Appendix 2.4), resulted in very abrupt steps, and even for dielectric coatings up to 1.5 times the lower electrode thickness, a step discontinuity existed in the dielectric (figure 7.2) which would ultimately lead, in the worst case, to a complete dielectric discontinuity and pinholes at the overlay (figure 7.8), and at best to low-voltage breakdown at the step.

The profile could be significantly improved using dip-etching techniques and ferric chloride as the etchant (Appendix 2.4) and allowing the lower electrode to be severely undercut. This then resulted in a bevelled lower electrode edge profile, which allowed a continuous coating of dielectric over the metal electrode step (figure 7.1). This processing technique was therefore adopted as standard for the remainder of the project.

Using the improved lower electrode profile, it was found that for silicon dioxide capacitors, the ratio of $\frac{\text{dielectric thickness}}{\text{lower electrode thickness}}$ could be decreased from 2.3 to 0.55 approximately, without any apparent increase in the % of pinholes occurring at the overlay (figure 7.9.a). Therefore, within these thickness ratio limits, and assuming the improved lower electrode profile, there is no indication that a minimum $\frac{\text{dielectric thickness}}{\text{lower electrode thickness}}$ ratio is required to achieve tolerable processing yields.

No data is available correlating the voltage breakdown and the ratio of $\frac{\text{dielectric thickness}}{\text{lower electrode thickness}}$, nor for the corresponding characteristics of capacitors with the 'abrupt' lower electrode profiles.

It was also noted (figure 7.9.b), that the dielectric thickness could be reduced to 0.6 μm without any apparent increase in the total number of pinholes in the film. It is therefore concluded that the dominating factor contributing to pinholes in silicon dioxide, for the lower electrode and dielectric thicknesses and profiles indicated above, is not the characteristics of the capacitor or dielectric as such,

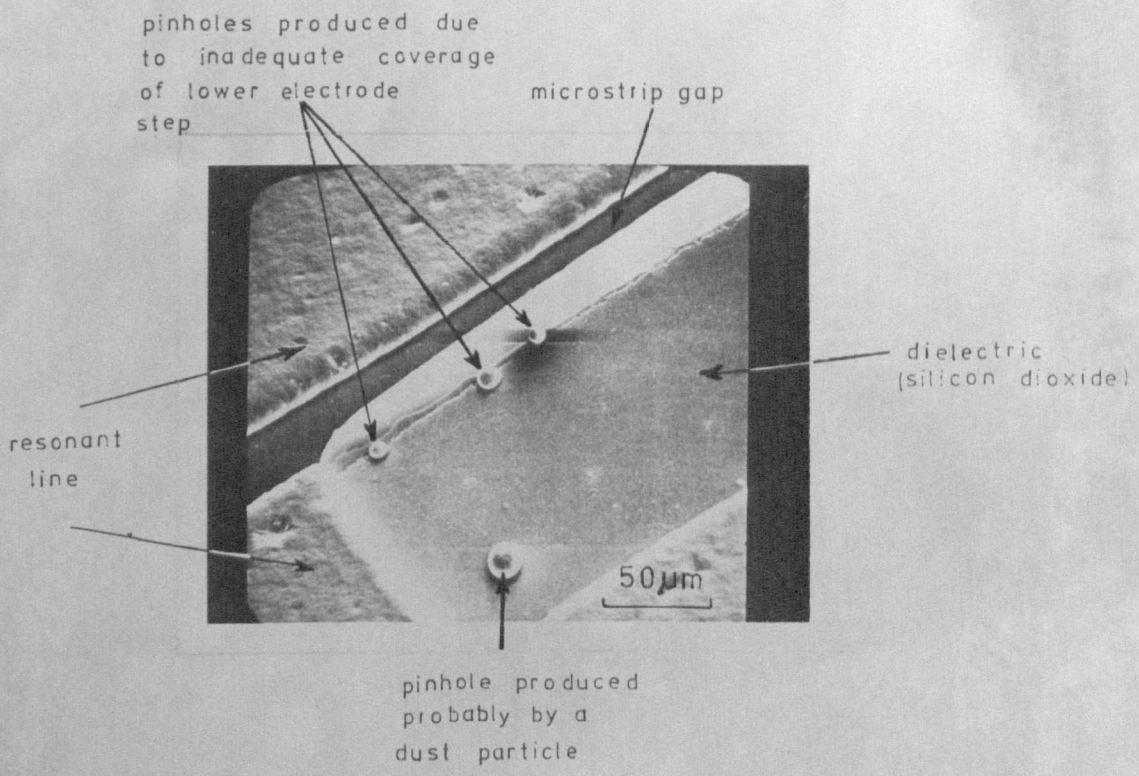
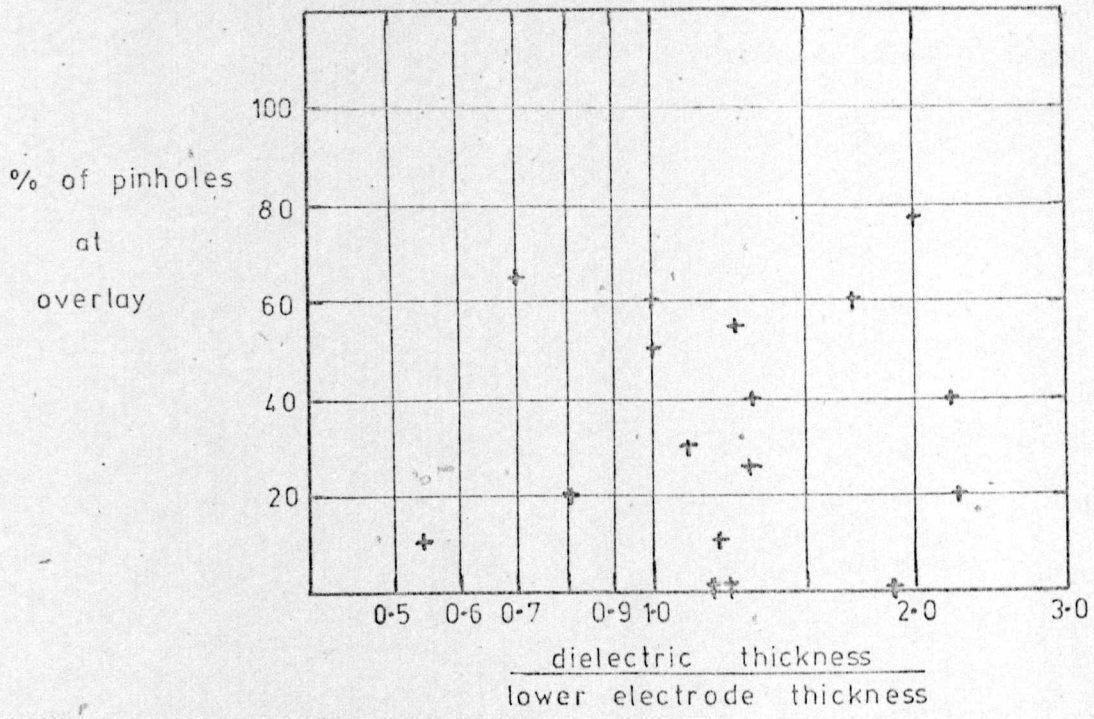
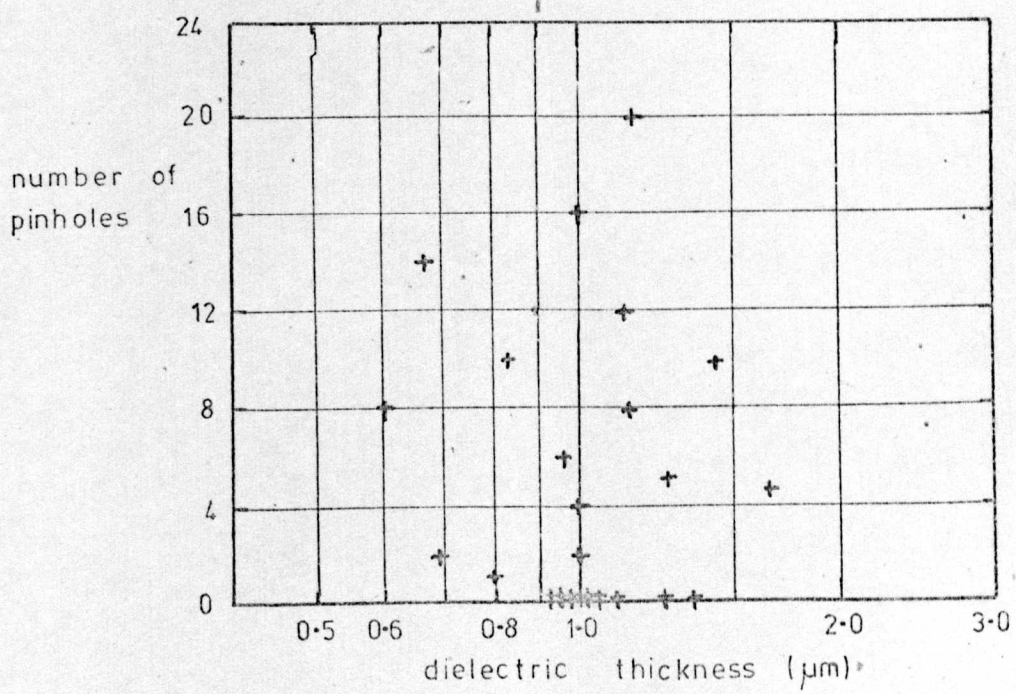


Figure 7·8 Pinholes disclosed in the dielectric after "plating-up" the resonant line.



(a) Effect of the ratio $\frac{\text{dielectric thickness}}{\text{lower electrode thickness}}$ on the % of pinholes occurring at the overlay



(b) Effect of the dielectric thickness on the number of pinholes

Figure 7·9 Pinhole analysis of silicon dioxide films

but more likely contamination during the processing.

Having improved the processing techniques to such a degree that silicon dioxide capacitors could be produced with a yield approaching 75%, identical techniques were applied to alumina technology. Immediately, however, the yields dropped to almost zero level ($\approx 5\%$), which was not due to processing factors alone, as a return to silicon dioxide technology immediately restored the yields to 75% approximately.

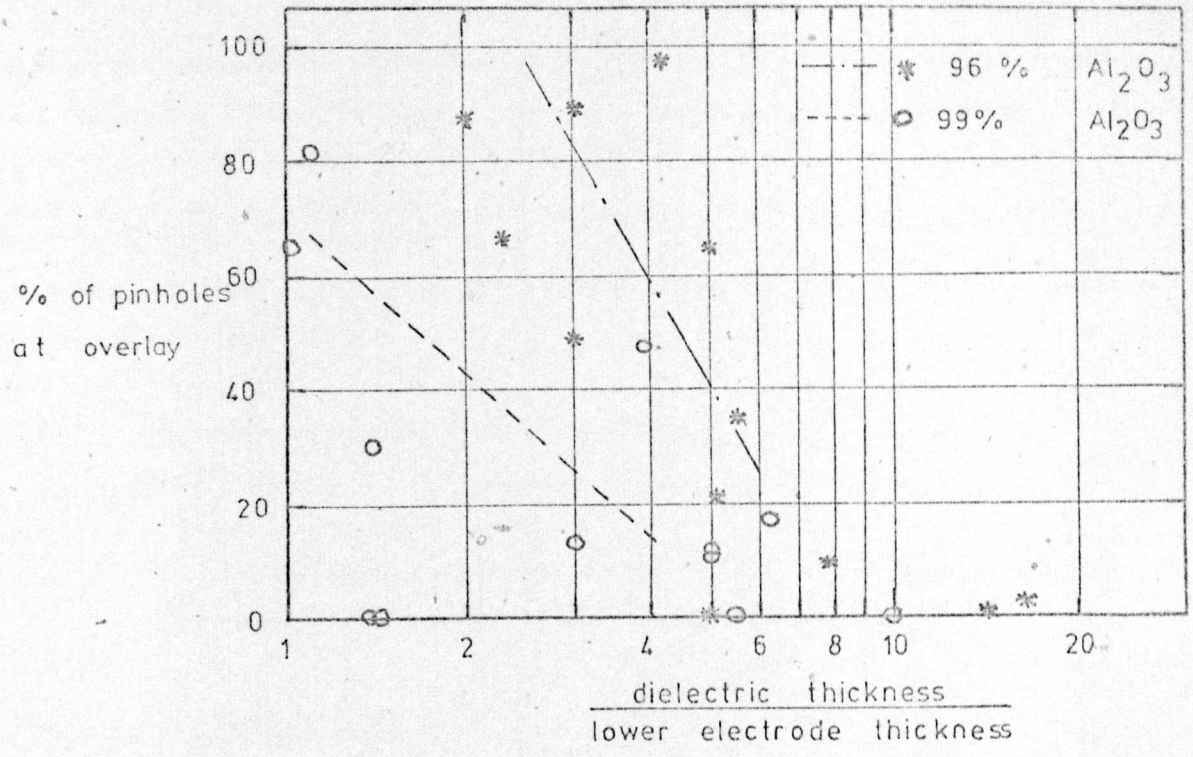
To isolate the cause of the increase in pinhole density, the effect of the $\frac{\text{dielectric thickness}}{\text{lower electrode thickness}}$ ratio on the % of pinholes at the overlay for alumina films, was investigated. The resulting data (figure 7.10.a) indicates a correlation between the % of pinholes at the overlay, and the thickness ratio, and the % of pinholes decreases as the ratio increases. This is in contrast to the results for silicon dioxide films, which indicated no such correlation.

It is also shown that for the lower quality alumina (i.e. 96%), the % of pinholes at the overlay is higher, for a given $\frac{\text{dielectric thickness}}{\text{lower electrode thickness}}$ ratio, than for the higher (99%) quality films.

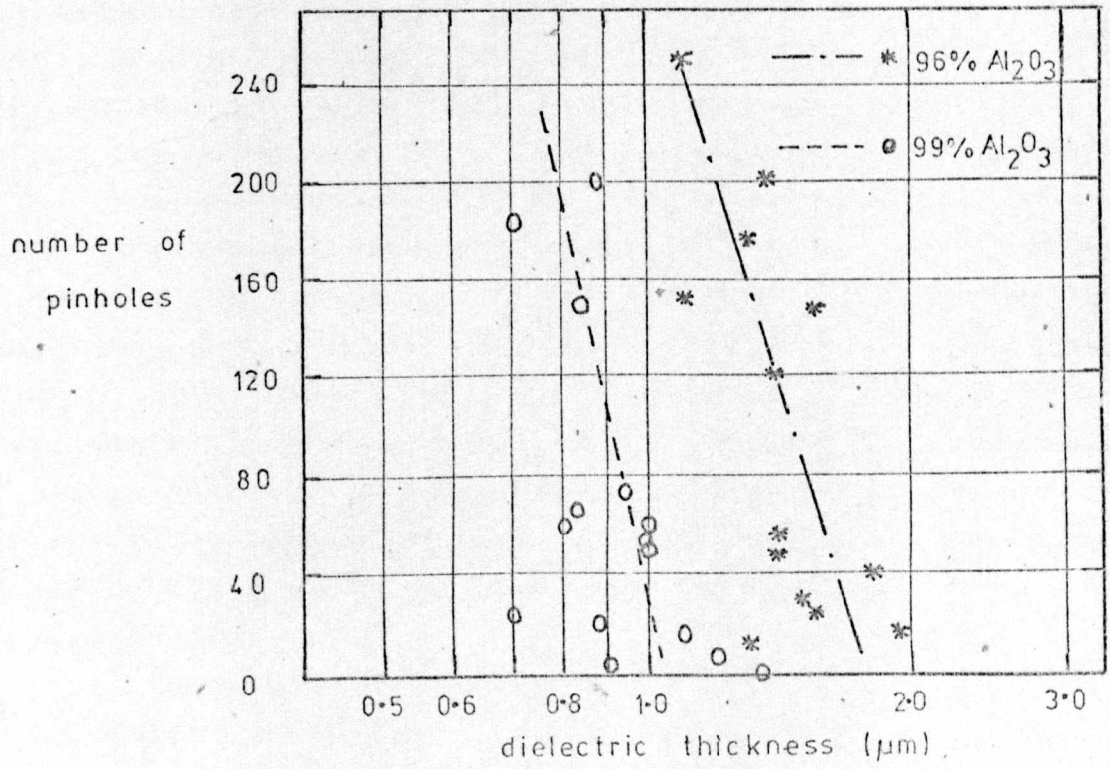
Figure 7.10.b, indicating the total number of pinholes as a function of the dielectric thickness, indicates a decrease in the number of pinholes as the dielectric thickness is increased, which was not evident in the case of silicon dioxide films. This figure also shows that the total number of pinholes increases as the dielectric quality decreases. This factor is further emphasised when a comparison is made between the total pinhole count for silicon dioxide films and alumina films, as the former is generally accepted as being of much higher quality than the latter.

This therefore indicates that the quality and density of the sputtered deposit is of major significance in the formation of pinholes in dielectric films, and that the capacitor characteristics (such as dielectric thickness and $\frac{\text{dielectric thickness}}{\text{lower electrode thickness}}$ ratio) only serve to augment basic deficiencies in the dielectric films.

In conclusion, therefore, from the studies described



(a) Effect of the ratio of $\frac{\text{dielectric thickness}}{\text{lower electrode thickness}}$ on the % of pinholes occurring at the overlay.



(b) The effect of dielectric thickness on the number of pinholes

Figure 7·10 Pinhole analysis of alumina films

above, the factors affecting the formation of pinholes in both silicon dioxide and alumina films (for dielectric thicknesses of between 0.6 μm and 2 μm, and for $\frac{\text{dielectric thickness}}{\text{lower electrode thickness}}$ ratios of between 0.5 and 2.5 for silicon dioxide, and between 1 and 20 for alumina) are, in order of importance

1. purity of sputtered material
2. dust count of environment
3. lower electrode profile
4. dielectric thickness, and the ratio of dielectric thickness to lower electrode thickness.

7.6.2 Processing yield.

The yield of capacitors, and test resonators with capacitors inserted, obtained throughout the project, was determined largely by the expertise of the operator, which improved as the number of batches processed increased. This was only the case, however, if all the batches considered were processed within a short time span of each other, as it was found that the yield dropped drastically if the time-lag between batches (the defamiliarisation time) was in excess of 2 - 3 weeks. The only significance of this is in the decrease in useful processing time experienced, which is not representative of a normal production environment.

At the outset, and considering the factors mentioned above, the circuit yield was non-existent due to a variety of defects e.g. pinholes, microstrip gaps not cleanly etched, microstrip gaps shorting during plating, cracked substrates. However, with improvements in the processing, the overall yield was greatly improved, and rejects were limited entirely to the presence of pinholes in the dielectric, with other factors being insignificant. Overall yield was therefore approximately 75% for silicon dioxide films, and 5% for alumina films.

To obtain these yields, however, it was found to be absolutely essential to inspect each substrate after every processing stage, and to rework or reject circuits

as required, at the earliest possible stage. In general it was found that faults accumulated throughout the process, making the further processing of slightly imperfect circuits an unprofitable procedure.

Improvements in the yield can only therefore be made by reducing the number of pinholes encountered in the dielectric films, as discussed in section 7.6.1. For silicon dioxide films, this involves decreasing the contamination from the environment during processing. For alumina films, the ultimate requirement is an increase in the quality of sputtering targets, but a possible solution, not verified at this stage, is to significantly increase the minimum dielectric thickness. This will decrease the available capacitance/unit area, but this effect is reduced in importance due to the relatively high dielectric constant.

7.7 Conclusions.

In this chapter it has been shown that overlay capacitors can be fabricated successfully (figures 7.11 and 7.12).

In addition, the processing techniques for overlay capacitors with copper or gold electrodes, and with any sputtered, or vacuum deposited, dielectric material, have been described.

The major conclusions drawn are

1. using the techniques described, silicon dioxide capacitors can be produced with a yield approaching 75%, and alumina capacitors with a yield of 5%.

2. the major contributing factor to the poor yield is the density of pinholes, which is caused by

   a) poor quality dielectric targets
   b) the high dust count of the processing environment
   c) abrupt lower electrode edge profiles
   d) too thin a dielectric layer

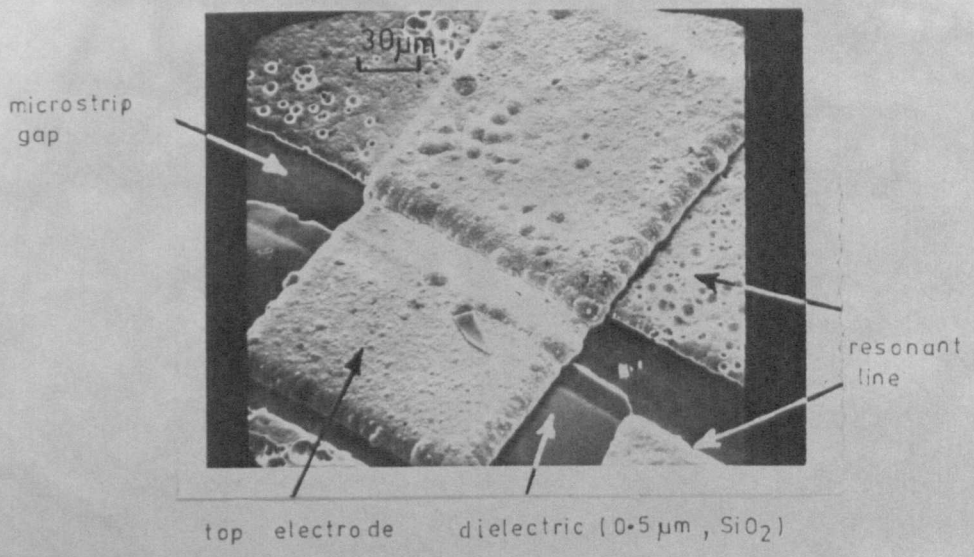


Figure 7·11 Prototype 0·5pF silicon dioxide capacitor

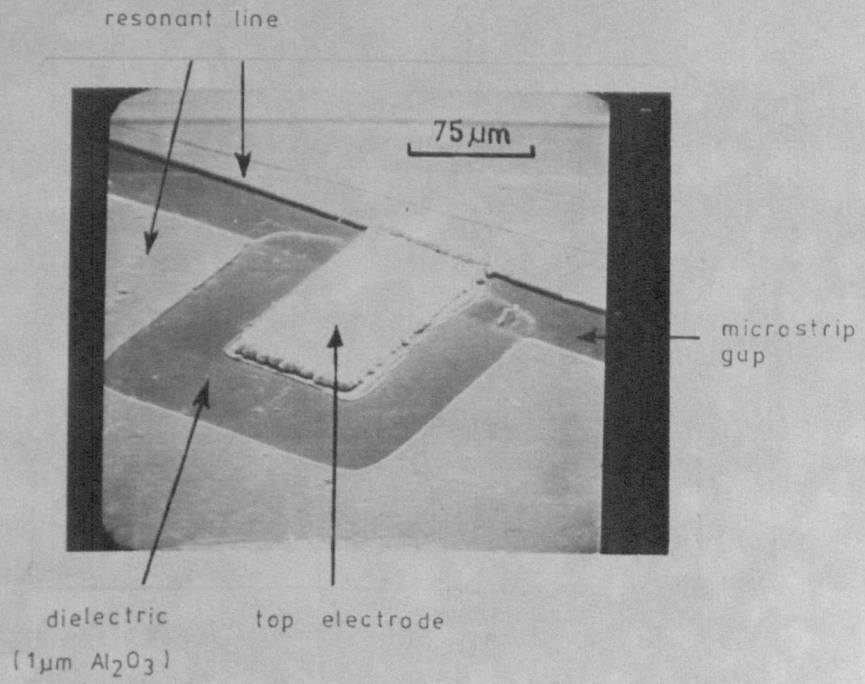


Figure 7·12 0·5pF alumina capacitor

e) the ratio of $\frac{\text{dielectric thickness}}{\text{lower electrode thickness}}$ being too low.

3. for silicon dioxide capacitors, dielectric thicknesses as low as 0.5 μm, and ratios of dielectric thickness to lower electrode thickness as low as 0.6, may be used without decreasing the yield.

4. for alumina capacitors, the dielectric thickness should be in excess of 2 μm, and the ratio of dielectric thickness to lower electrode thickness should be as large as practical if yields in excess of 5% are to be achieved.

8. A PRACTICAL MEASUREMENT SYSTEM FOR OVERLAY CAPACITORS.

8.1 Introduction.

In Chapters 5 and 6, the theory of a measurement technique for the evaluation of the properties of overlay capacitors was presented. In this chapter, these theories are extended into a practical measurement system, and in particular, emphasis is placed on

1) a description of the measurement procedure,
2) a verification of the correctness of the theoretical analysis of the measurement technique described in Chapter 5,
3) an estimation of the overall measurement system accuracy.

8.2 Measurement procedure.

8.2.1 Introduction.

The measurement equipment used to determine the microwave properties of the test resonators, is a waveguide reflectometer (figure 8.1). The measured resonator parameters (i.e. the frequency, return loss and Q factor at resonance), and the characteristics of the resonators already determined from previous measurements (e.g. the gap capacitors, C_c and C_g, measured in Chapter 4), permit several different methods for the evaluation of the desired capacitor properties (i.e. the capacitance and Q factor). This section outlines the main factors which contributed to the selection of the method finally adopted, and in addition, presents a comprehensive schedule of the complete measurement procedure.

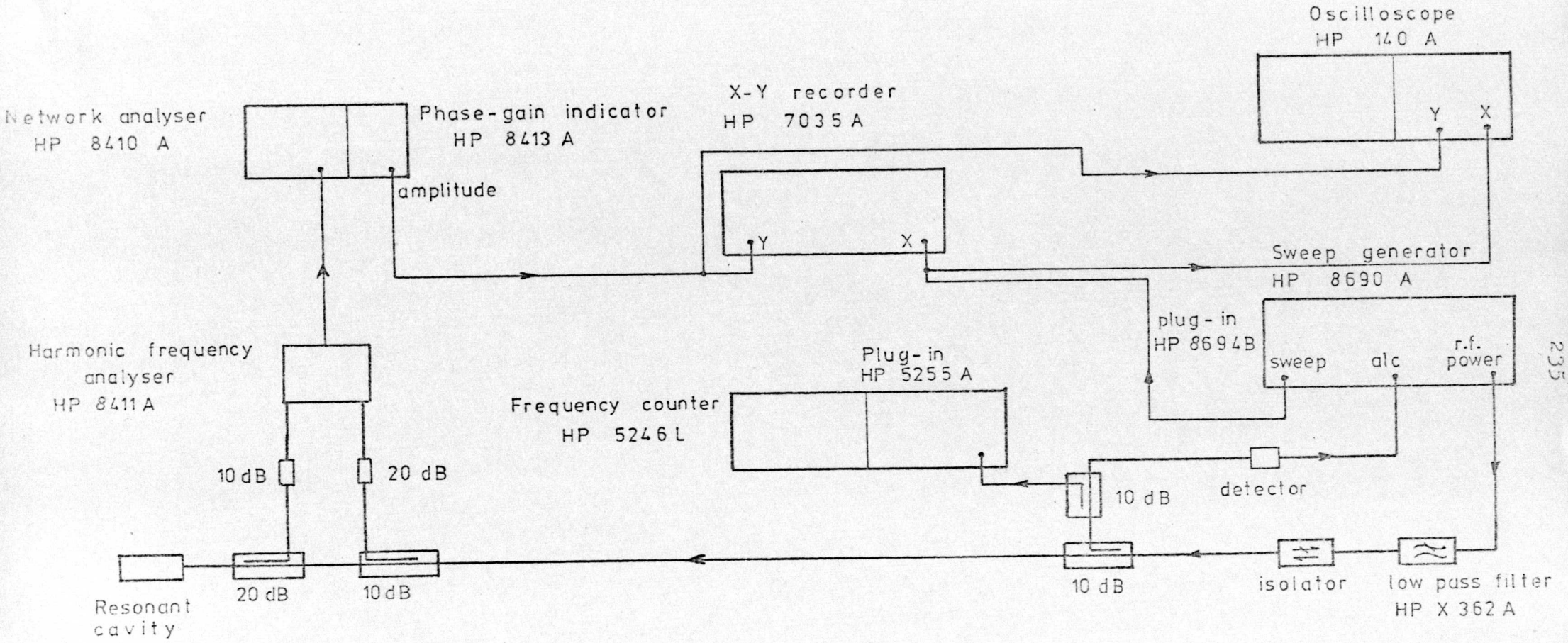


Figure 8·1.a X Band Waveguide Reflectometer

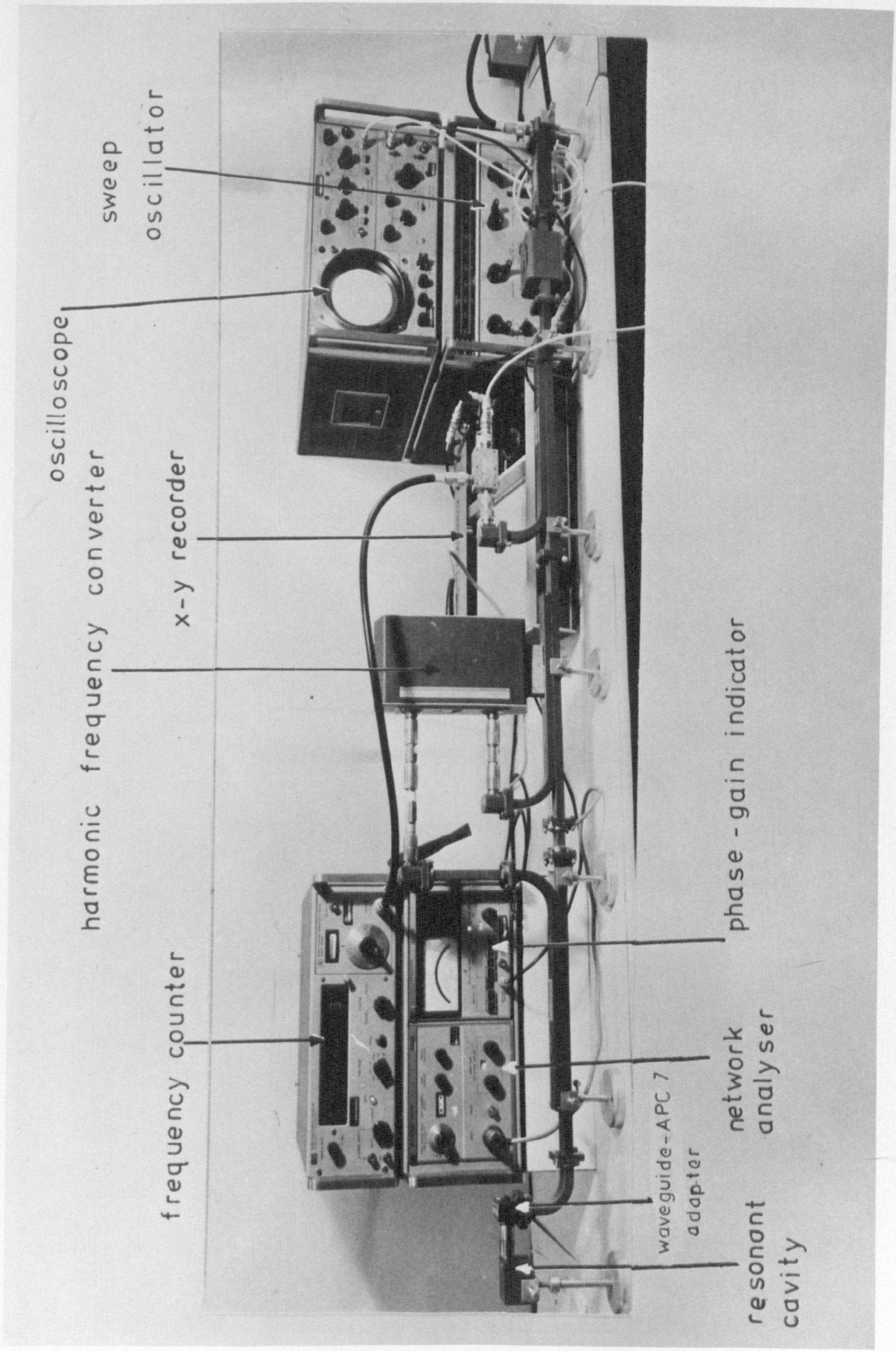


Figure 8-1-b Waveguide reflectometer

8.2.2 Selection of the measurement procedure.

Limitations of the processing techniques.

In prototype resonators, the widths of the microstrip gaps were found to vary by typically ± 2.5 μm across the width of the resonant line, due to variations in the processing techniques.

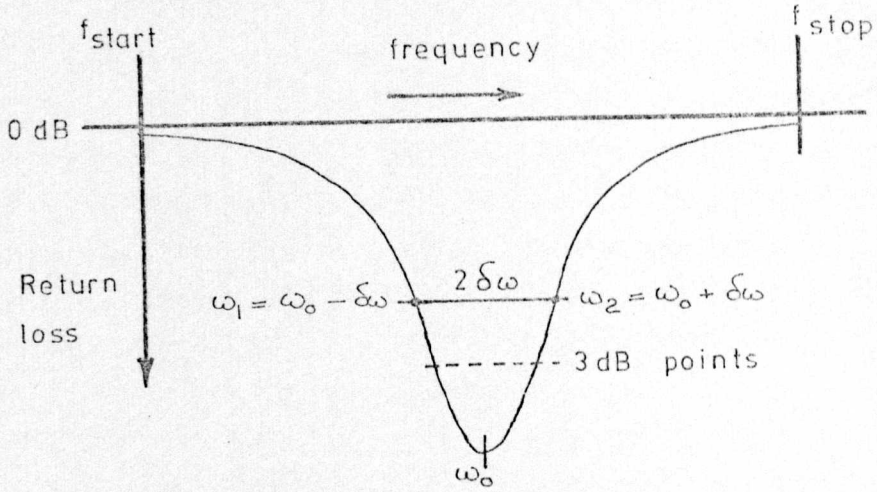
For this reason, it was considered preferable in the overlay capacitor measurement technique, to measure the gap capacitors, C_g and C_c, for each resonator, and not to utilise the previously tabulated data of figures 4.17 and 4.23.

The methods of measurement of these capacitors are described in detail in section 8.2.3. Capacitor values determined using these methods are shown (figures 4.17 and 4.23) to agree closely with capacitor values determined using the previously described techniques of Chapter 4.

Limitations on the accuracy of Q factor measurement.

The method used for the measurement of the resonator Q factor (Appendix 8.1), which was found to be the most accurate of the methods available to the author (Appendix 8.4), requires a plot of the return loss as a function of frequency about resonance (figure 8.2), and the measurement, from this plot, of the return loss at 3 discrete frequencies. The return loss measurements are made with respect to the 0 dB reference level, and due to multiple reflections in the reflectometer system, the reference level varies as a function of frequency (figure 8.3), and introduces an error of Δ dB in each of the three return loss measurements. Although this error has been reduced to a minimum (0.09 dB for a 100 MHz sweep), by careful selection of the reflectometer components (Appendix 8.4), it nevertheless places a fundamental limitation on the accuracy of Q factor measurement.

The effects of this error on the measured capacitor properties could be significantly reduced if measurements of the return loss were made only at one frequency. This method is possible, if the return loss at resonance is



ω_0 = resonant frequency

ω_1, ω_2 = lower and upper bandwidth points

f_{start}, f_{stop} = frequency sweep start and stop frequencies

Figure 8·2 Resonance plot for the measurement of Q factor.

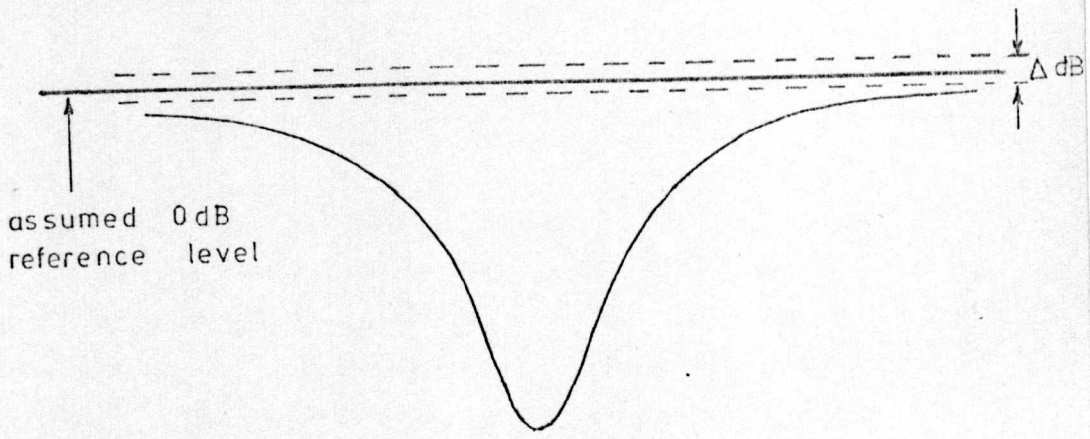


Figure 8·3 Return loss plot showing the error (Δ dB) associated with the 0 dB reference level.

measured, and the coupling capacitor, C_c, is accurately known. As has been established previously, the coupling capacitance will be determined from measurements of the return loss, Q factor, and resonant frequency of the basic resonator, without the test capacitor inserted. Therefore, using the calculated value of coupling capacitance, and the return loss at resonance (measured using the reflectometer of figure 8.1), the resonator losses can be determined.

Similarly, from measurements of the return loss at resonance of the resonator with the test capacitor inserted, the capacitor losses can be evaluated.

In addition to the direct advantages of increased accuracy by using the return loss measurements in preference to the Q factor measurements, the measurements of the return loss can be performed much more quickly than the corresponding Q factor measurements, as only a small section of the return loss - frequency plot (i.e. around resonance) is required. Hence more measurements can be made in a given time, and a higher level of confidence in the results can be achieved.

8.2.3 Measurement procedure.

A comprehensive schedule for the measurement procedure is given in Appendix 8.5, and will not, therefore, be repeated at this stage.

To increase the overall accuracy of measurement of the resonator and capacitor properties, and to reduce the possibility of spurious measurement errors, a series of measurements was performed on each test resonator.

For the basic resonator, without the test capacitor inserted, 5 measurements of the return loss at resonance, and 1 measurement of the Q factor, were made. The test resonator was then completely removed from the shielding enclosure, replaced, and the measurements were repeated. This complete procedure was repeated a total of 5 times, resulting in a total of 25 return loss measurements and 5 Q factor measurements, from which a mean set of results could be obtained.

For the resonator with the test capacitor inserted,

the measurement procedure was similar, with the exception that the Q factor measurements were ignored.

8.2.4 Analysis of the measurement data.

Due to the number and complexity of the calculations involved in the determination of the overlay capacitor characteristics, the computations were performed by computer.

The computer program is based fundamentally on the flow diagram given in Appendix 8.5, and a more detailed program flow diagram, giving the procedure for each of the individual calculations, is given in Appendix 8.6.

The program listing is given in Appendix 8.7, and a print-out of typical results is given in Appendix 8.8.

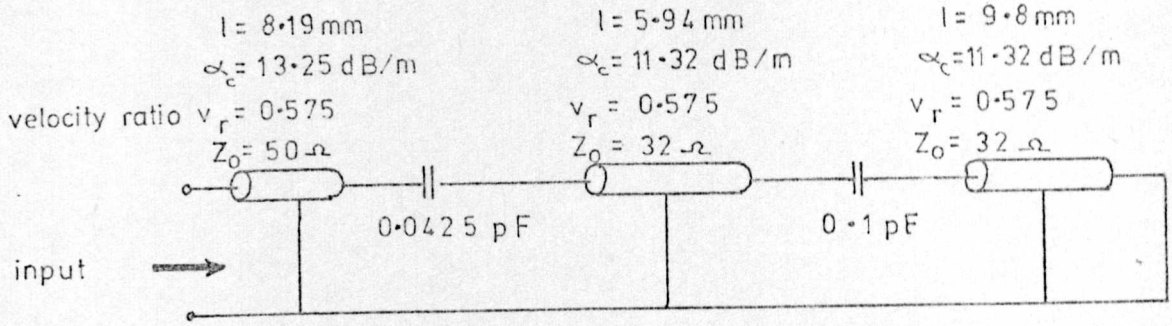
8.3 Verification of the measurement technique accuracy.

8.3.1 Verification of the theoretical analysis.

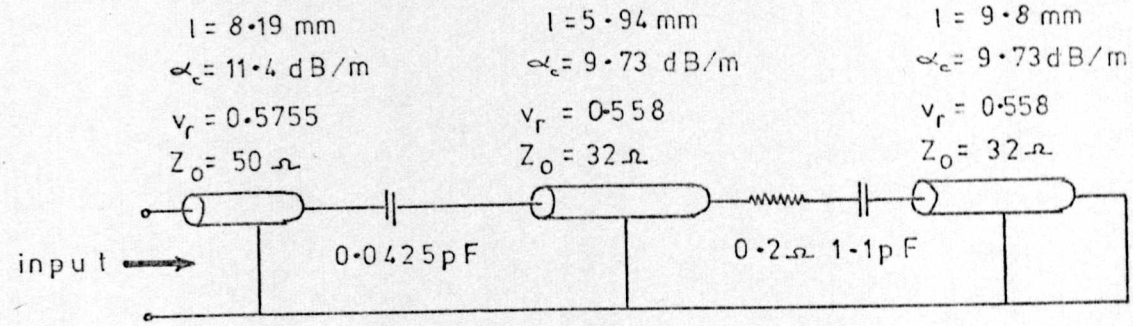
To enable both the measurement technique and the computer program to be used with confidence, it was considered essential to perform a systematic check of the complete measurement system before any microwave capacitors were measured. This was achieved by simulating the complete measurement technique on the computer, using the circuit anan**Lysis** programs of Marchent [172].

The test procedure consisted of formulating the equivalent circuits of typical resonators at each of the measurement stages (i.e. without and with the test capacitor inserted - figures 8.4.a and 8.4.b, respectively), and calculating the input impedance using Marchent's programs, as the frequency is swept from 8 - 12 GHz. From the programs, the input impedance data was obtained in two forms

a) S_{11} in dB and phase - equivalent to the output of the phase - gain indicator of the reflectometer. Hence, a plot of return loss versus frequency could be obtained for both of the resonator circuits (figure 8.5).

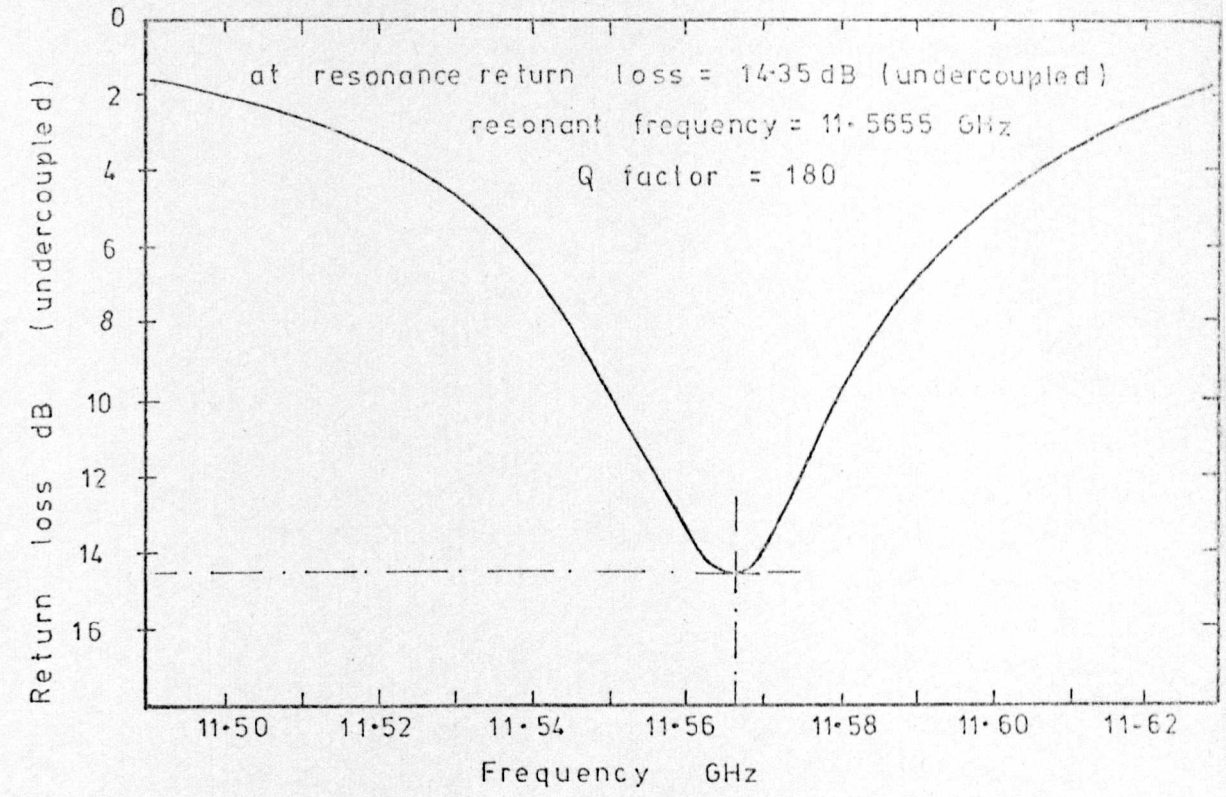


(a) Without test capacitor inserted

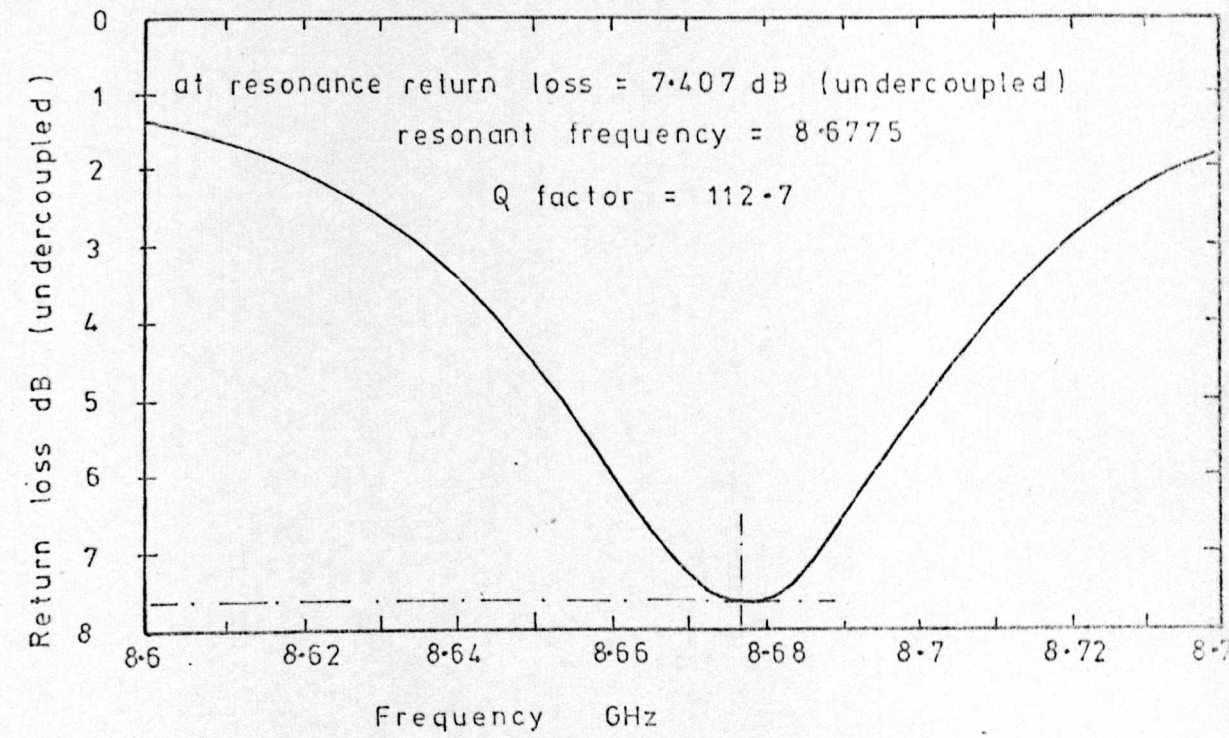


(b) With test capacitor inserted

Figure 8·4 Test circuits used to test the correctness of the measurement circuit theoretical analysis, and the computer program.



(a) Measurement without the test capacitor inserted



(b) Measurement with the test capacitor inserted

Figure 8·5 Simulated return loss - frequency plots obtained by computer analysis of the equivalent circuits of figure 8·4.

b) S_{11} in modulus and argument - equivalent to the output of the polar display unit of the reflectometer. Hence, a polar plot of the resonances can be obtained (figure 8.6).

Therefore, the output data obtained from the program of Marchent is identical to that which can be obtained from the practical microwave measurements using the reflectometer.

From the resulting plots of figures 8.5 and 8.6, the return loss at resonance, the Q factor and the resonant frequency could be determined for both measurements in turn, in identical methods to those used for the practical measurements.

This information, together with the known resonator dimensions, was then used as data for the measurement analysis program of Appendix 8.7, and the effective capacitance, C*, and the effective capacitor Q factor, Q*, were calculated. The resulting calculated data, and the original parameters, are compared in figure 8.7, and hence an indication of the correctness of the measurement technique can be achieved.

The values of conductor attenuation adopted in the test circuits were typical of those exhibited by the prototype, low Q factor, resonators ($Q \approx 250$). The values of the Q factor, return loss, and coupling capacitance thus obtained cannot, therefore, be directly compared with those of the final resonators, in which the Q factor approached 400.

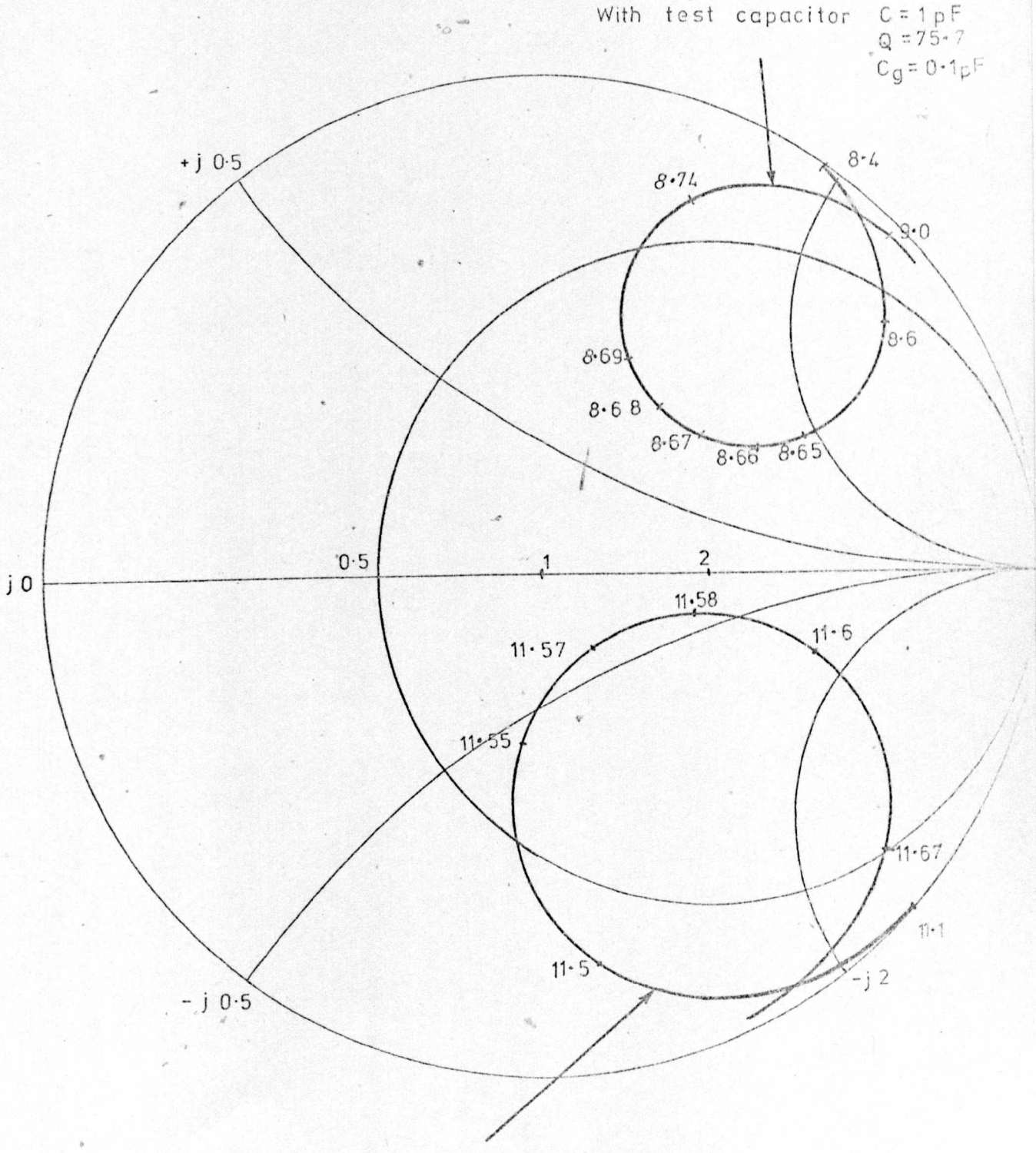
This does not, however, detract from the usefulness of the simulation, in verifying the correctness of the theoretical analysis of the measurement technique, and in verifying the correctness of the measurement analysis computer program.

From the results (figure 8.7), it will be noted that for each measurement, only one resonance exists in X band. For the initial measurement, without the test capacitor, this resonance occurs at 11.5655 GHz, and for the second measurement, with the test capacitor, the resonant frequency is 8.6775 GHz. It will be observed that for the circuit configuration described, the resonant frequencies agree well with the design curve shown in figure 5.10.

It will also be noted that the resonant frequency for the second measurement is sufficiently far removed from

Figure 8·6

Simulated resonance plots obtained by computer analysis of the equivalent circuits of figure 8·4



Simulated measurement	Number of resonances in X band	Resonant frequency GHz	Return loss dB	Q factor
Without test capacitor	1	11.5655	14.35 (under-coupled)	180
With test capacitor	1	8.6775	7.407 (under-coupled)	112.7

a) Simulated measured microwave resonator properties.

Parameter	Theoretical	Simulated measured	Deviation %
Coupling capacitance C_c	0.0425pF	0.0431pF	1.4%
gap capacitance	0.1pF	0.103pF	3.0%
test capacitance	1.0pF	0.993pF	0.7%
test capacitor Q factor	75.7	75.72	0.027%

b) Actual and simulated measured data for the test capacitor.

Figure 8·7 Microwave measurement technique evaluation.

the anticipated box resonance at 8.2 GHz to avoid multiple resonance difficulties.

It will also be observed that the values of return loss obtained agree well with those predicted from figures 5.25 and 5.26.

A noticeable feature of figure 8.6 is that both resonances are symmetrically displaced about a point of high impedance (i.e. a point of low current density). This minimises some of the difficulties encountered in the reproducibility of earlier measurements, of making electrical contact at a point of high current density.

The most significant data obtained from the simulation exercise is to be found in figure 8.7.b, which compares the calculated capacitor parameters with the known values incorporated in the original equivalent circuit. From this it can be seen that the test capacitance is calculated to within 0.7%, and the capacitor Q value to within 0.027%, which amply demonstrates that the theoretical analysis of the resonator technique, and the computer program for the calculation of the characteristics from the measured data, are functioning as designed.

8.3.2 The effect of the additional processing stages on the resonator properties.

One of the features of the measurement technique described, is that the resonant line undergoes additional processing stages between the measurement of its properties, and the measurement of the composite properties of the test capacitor and the resonator, and it is essential that the resonator properties themselves are not affected by the additional processing stages.

To ensure that this was, in fact, the case, three resonant lines were processed using the normal processing techniques (Appendix 7.1, stages 1 - 24), and the line properties were measured by the normal methods. The additional stages (Appendix 7.1, stages 25 - 32), for the formation of the top electrode were then performed, with the exception of the exposure of the top electrode mask (stage 27). In this particular case, the complete substrate (completely

coated with negative resist) was exposed to ultraviolet light. This resulted in these particular substrates being exposed to exactly the same processing environment as the normal test resonators, but without the top electrode actually being formed. The resonators were then, fundamentally, unchanged from the initial measurements, apart from any changes in the characteristics encountered as a result of the additional processing stages to which the resonators have been exposed.

The resonator properties were then, once again, measured by the normal method, and the results, shown in figure 8.8, indicate conclusively, that any changes in the resonator properties due to the additional processing stages, are in fact within the variations expected from the overall measurement technique accuracy.

It is concluded, therefore, that the additional processing stages have no effect on the measured resonator properties.

8.4 Error analysis of the measurement technique.

Due to the complexity of the calculations of the test capacitance and the Q factor, the evaluation of the measurement system accuracy, using conventional differential techniques, is impractical.

However, the effect of small errors in the measured parameters on the error in the calculated test capacitance and Q factor, were calculated using the measurement analysis computer program of Appendix 8.7, and are displayed in figures 8.9.a and 8.9.b respectively. The overall accuracy of measurement of the test capacitance and Q factor, were then determined (figure 8.10) from the numerical sum of the individual error contributions, which indicates a worst - case error, as compensating errors are not taken into account.

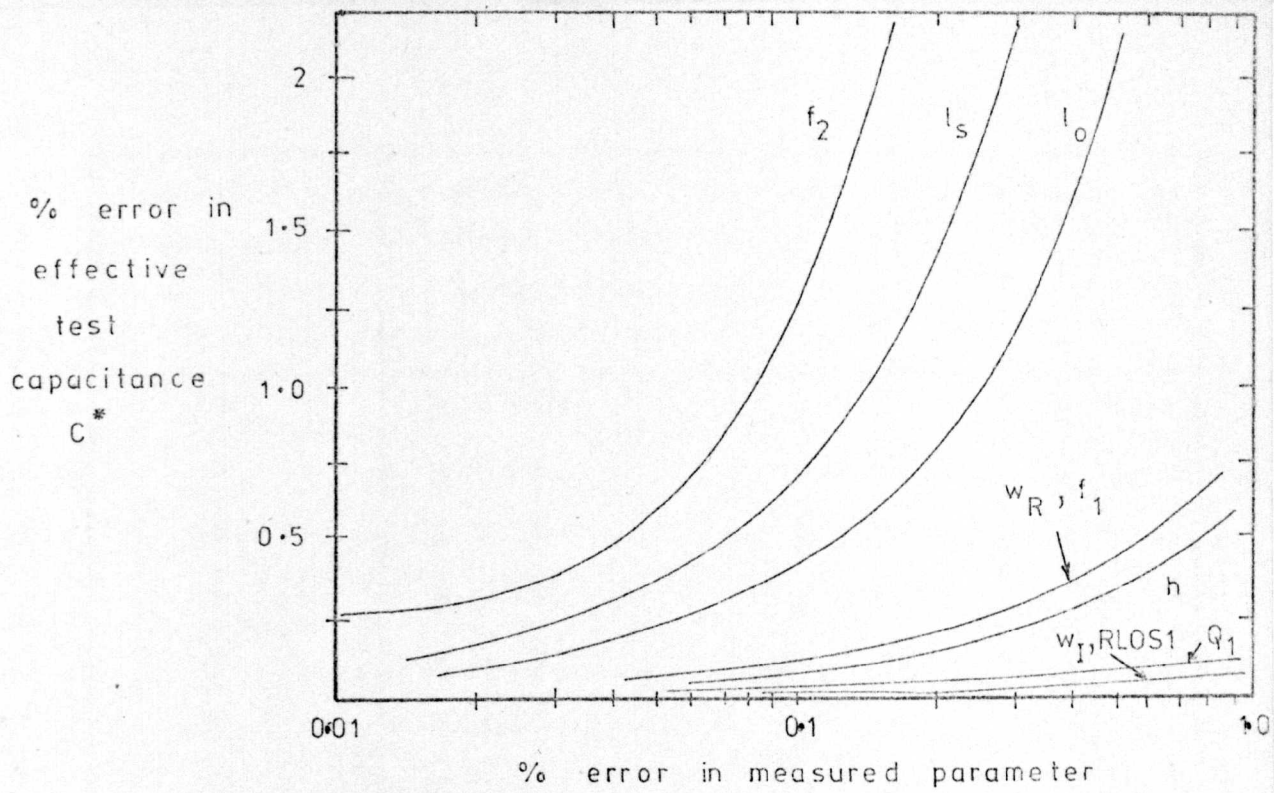
The results indicate worst - case errors of

$\pm$ 1.025 % for the effective capacitance, C*, and

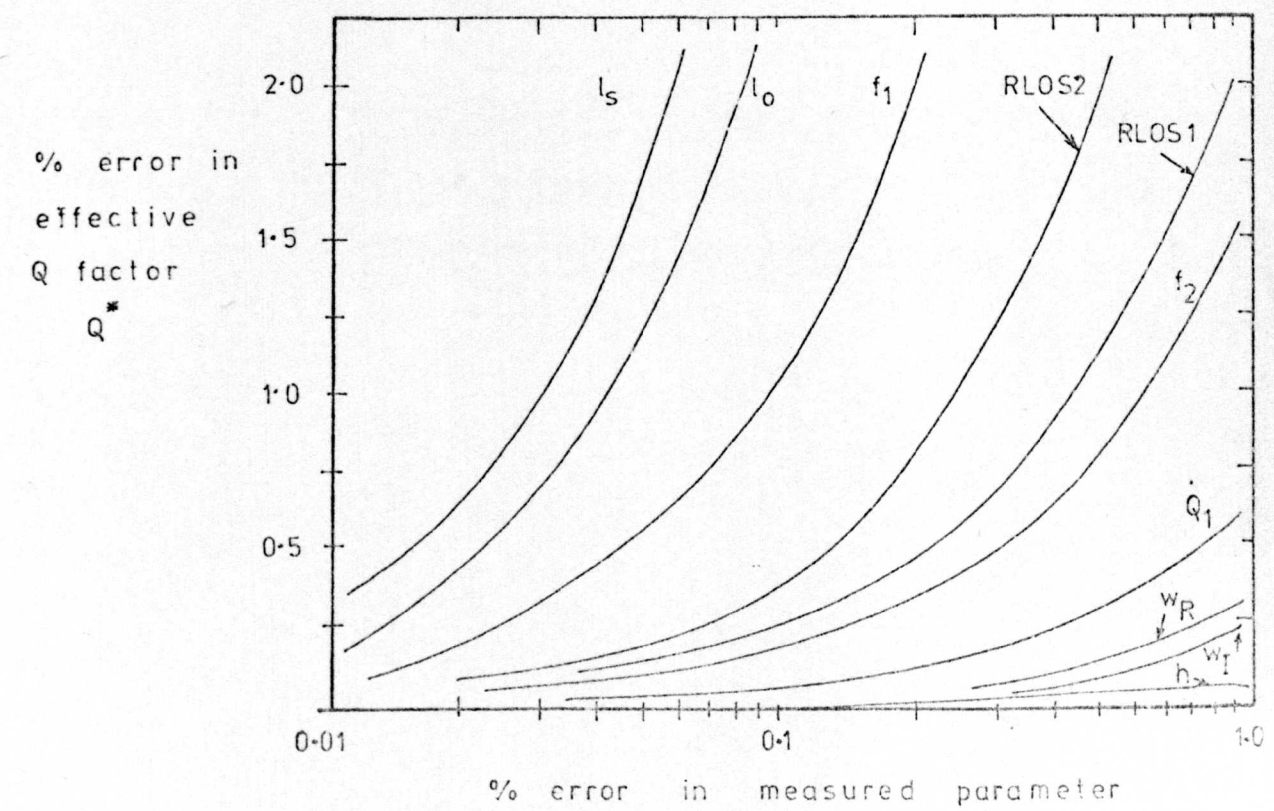
$\pm$ 7.2 % for the effective capacitor Q factor, Q*.

Sample	INITIAL MEASUREMENTS			MEASUREMENTS AFTER ADDITIONAL PROCESSING STAGES			VARIANCE %		
	Resonant frequency GHz	Return loss dB	Q factor	Resonant frequency GHz	Return loss dB	Q factor	Resonant frequency	Return loss	Q factor
1	11·81173	27·3	250·7	11·81091	27·42	252·45	- 0·007	+0·44	+ 0·66
2	11·77725	25·75	235·2	11·77753	25·69	233·8	+ 0·0025	- 0·23	- 0·60
3	11·79137	25·97	245·6	11·79179	25·86	243·7	+ 0·0037	- 0·42	- 0·77

Figure 8·8 The effect of the additional processing stages on the microwave properties of the test resonators.



a) Error in effective test capacitance C^*



b) Error in effective Q factor Q^*

Figure 8·9 Contributions to the errors in the calculated capacitor properties, C^* and Q^*, of errors in the individual measured parameters.

Parameter	Practical measurement accuracy %	Contribution to error	
		Capacitance %	Q %
l_s	± 0.025	± 0.2	± 0.85
l_o	± 0.04	± 0.15	± 1.0
w_I	± 0.25	± 0.00	± 0.05
w_R	± 0.125	± 0.1	± 0.025
f_1	± 0.01	± 0.025	± 0.1
f_2	± 0.01	± 0.025	± 0.025
Q_1	± 0.8	± 0.075	± 0.5
RLOS1	± 0.7	± 0.025	± 1.85
RLOS2	± 0.7	± 0.00	± 2.75
h	± 0.3	± 0.2	± 0.05
Total error		± 1.025%	± 7.2%

Figure 8·10 Error analysis of the microwave measurement of the effective capacitance, C*, and the effective capacitor Q factor, Q*.

8.5 Conclusions.

In this Chapter, the overall practical measurement procedure involved in the determination of the properties of microwave overlay capacitors has been described in detail, and the calculations involved in the evaluation of the capacitor properties have been outlined.

A flow diagram, and a program listing, of the computer program used to determine the capacitor properties from the measured microwave parameters, are also documented.

It has been verified, by computer simulation techniques, that the theoretical analysis of the resonator technique described in Chapter 5, and the measurement analysis program, are fundamentally correct.

It has also been shown that the processing stages incorporated between the two microwave measurements, have no effect on the resonator properties themselves, and therefore any difference in the microwave properties of the two measurements, are attributed entirely to the presence of the test capacitor.

It has also been shown that the worst-case errors in the measured capacitor properties are $\pm$ 1.025% for the effective capacitance, C*, and $\pm$ 7.2% for the effective Q factor, Q*.

9. MEASUREMENTS ON MICROWAVE OVERLAY CAPACITORS.

9.1 Introduction.

This chapter presents the results of measurements performed by the author, on microwave overlay capacitors using the techniques described in the preceding chapters.

As a consequence of the low processing yields experienced with alumina dielectric materials, most of the measurements refer to silicon dioxide capacitors.

To a very limited extent, both the geometrical parameters of the capacitors, and the dielectric deposition conditions, have been varied to indicate the relative effects on the performance of the capacitors.

The measurement results obtained are compared with the very limited published data available for similar measurements by other research workers. In addition, the properties of the capacitor dielectric materials derived from the author's capacitor measurements, are compared with the properties of the dielectrics in isolation, measured by Butlin[7] using cavity techniques.

9.2 Measurement results.

The results of measurements on 12 overlay capacitors are tabulated in figures 9.1 and 9.2. The microstrip resonator properties are tabulated in figure 9.1, and the overlay capacitor properties, which are measured at approximately 8.6 GHz, are given in figure 9.2.

From these results it can be seen that for 1 pF (nominal) capacitors, typical capacitor Q factors of between 125 and 150 with silicon dioxide as dielectric, and between 165 and 190 with alumina as dielectric, can readily be achieved.

The theoretical values of electrode Q factor, which have been calculated using Butlin's measured values of electrode material surface resistivity, are seen to be between 1000 and 2500, for capacitor aspect ratios (width/length)

OVERLAY CAPACITOR MEASUREMENTS Figure 9-1

SAMPLE	RESONATOR PHYSICAL PROPERTIES							MICROWAVE PROPERTIES						MEASURED GAP PROPERTIES	
	SUBSTRATE THICKNESS (m.m)	L_o (mm)	L_s (m.m)	W_I (m.m)	W_R (m.m)	COUPLING GAP WIDTH (μm)	CAPACITANCE GAP WIDTH (μm)	FREQUENCY (GHz)	Q_1	RETURN LOSS RLOS1 (dB)	FREQUENCY (GHz)	Q_2	RETURN LOSS RLOS2 (dB)	C_c PF	C_g PF
1	0·489	5·943	9·910	1·053	2·003	25·0	45·4	11·82847	350·0	+ 16·26	8·62082	219·1	-42·99	0·05	0·072
2	0·502	5·935	9·888	1·062	2·058	38·5	31·1	11·777119	393·0	+14·74	8·59942	232·7	-30·26	0·047	0·079
3	0·506	5·935	9·830	1·080	2·045	21·4	33·4	11·816152	375·0	+ 11·0	8·855785	230·8	+24·65	0·051	0·078
4	0·510	5·928	9·830	1·078	2·033	44·2	22·2	11·763321	347·0	+ 15·3	8·806320	217·5	-26·27	0·047	0·083
5	0·510	5·925	9·888	1·075	2·050	36·5	25·5	11·753631	400·1	+ 13·5	8·700327	229·6	-36·28	0·048	0·080
6	0·514	5·936	9·910	1·070	2·035	31·0	38·0	11·767638	341·0	+15·6	8·61529	212·7	-36·1	0·050	0·076
7	0·498	5·938	9·863	1·055	2·013	30·0	41·3	11·82687	372·0	+ 12·79	8·52869	230·3	+34·89	0·050	0·075
8	0·516	5·943	9·875	1·075	2·025	41·3	40·2	11·808772	395·0	+14·12	8·51954	237·9	-33·43	0·047	0·074
9	0·501	5·933	9·875	1·075	2·015	38·4	25·0	11·74022	347·0	+15·79	8·589310	215·4	-25·49	0·048	0·082
10	0·508	5·925	9·995	1·083	2·047	27·5	61·0	11·82197	383·0	+20·99	8·51328	238·8	+32·27	0·050	0·067
11	0·515	5·936	9·995	1·088	2·040	28·2	61·8	11·807619	389·0	+20·2	8·342625	260·4	+27·04	0·049	0·067
12	0·522	5·938	9·863	1·095	2·073	37·5	36·5	11·798279	365·0	+15·1	8·491157	238·8	- 36·10	0·047	0·077

OVERLAY CAPACITOR MEASUREMENTS Figure 9·2

SAMPLE	CAPACITOR PHYSICAL PROPERTIES									CAPACITOR MICROWAVE PROPERTIES							
	DIELECTRIC MATERIAL	DIELECTRIC THICKNESS (μm)	TOP ELECTRODE THICKNESS (μm)	LOWER ELECTRODE THICKNESS (μm)	CAPACITOR LENGTH l_3 (μm)	CAPACITOR WIDTH W (μm)	CAPACITOR ASPECT RATIO W/l_3	TOP ELECTRODE FEEDER LENGTH (μm)	LOWER ELECTRODE FEEDER LENGTH (μm)	EFFECTIVE CAPACITOR Q FACTOR Q^*	EFFECTIVE CAPACITANCE C^* pF	Parasitic Inductance L_3' nH	$\omega^2 L_3' C$ %	ACTUAL CAPACITANCE C pF	EFFECTIVE ELECTRODE Q FACTOR Q_E^*	ACTUAL DIELECTRIC Q FACTOR Q_D	DIELECTRIC CONSTANT ϵ_d
1	SiO_2	1·0	3·91	0·8	123	215	1·75	45·0	20·0	142·3	0·91	0·027	6·7	0·85	1573	168	3·64
2	SiO_2	1·02	4·87	0·82	131	229	1·75	28·0	16·0	130·0	0·96	0·017	4·6	0·92	1888	146	3·54
3	SiO_2	0·99	5·01	0·72	83	250	3·01	47·0	10·0	151·4	0·70	0·027	5·5	0·66	2284	172	3·58
4	SiO_2	1·35	4·98	0·79	131	228	1·74	22·0	22·0	147·2	0·75	0·013	2·9	0·73	2489	161	3·70
5	SiO_2	1·00	4·87	0·84	115	218	1·9	25·0	15·0	124·4	0·83	0·015	3·6	0·80	2311	136	3·62
6	SiO_2	1·1	4·52	0·51	125	240	1·92	32·5	22·0	136·5	0·90	0·019	4·8	0·86	1361	159	3·55
7	SiO_2	0·98	5·12	1·1	141·5	225	1·6	33·0	10·0	138·7	1·07	0·020	5·7	1·00	1779	160	3·50
8	SiO_2	0·96	5·01	0·5	137	219	1·6	35·0	17·0	132·6	1·06	0·021	6·0	0·99	1011	162	3·59
9	SiO_2	1·00	4·70	0·91	121	243	2·01	20·0	18·0	134·4	0·97	0·012	3·3	0·94	2392	147	3·60
10	SiO_2	1·26	4·68	1·1	125	300	2·4	55·5	17·5	147·8	1·02	0·031	8·2	0·93	1945	174	3·54
11	Al_2O_3	1·16	4·72	1·1	80	213	2·66	50·0	12·0	189·0	1·26	0·030	9·4	1·14	1465	240	8·75
12	Al_2O_3	1·06	4·27	0·79	74	191	2·58	30·0	20·0	167·5	1·12	0·019	5·7	1·06	1675	197	8·96

of between 1.6 and 3.0.

The values of dielectric Q factor, which are derived from these theoretical values of electrode Q factor and from the measured values of capacitor Q factor, are then predicted to be between 135 and 175 for silicon dioxide, and between 197 and 240 for alumina.

This then implies that the overall losses are determined primarily by the dielectric loss, with the electrode loss contributing substantially less by comparison.

It will be noted that the theoretical values of parasitic electrode inductive reactance, are less than 10% (and are on average 5.5%) of the capacitive reactance due to the dielectric. This then suggests that the effective capacitance will change, on average, by approximately 5% as the frequency is swept from 8 to 12 GHz.

The values of dielectric constants, which are determined from the theoretical values of electrode inductance and the measured values of effective capacitance, are then predicted to be 3.59 $\pm$ 0.06 for silicon dioxide (bulk value 3.78), and 8.86 for alumina (bulk value 9.6 - 9.9).

The closeness of these calculated values to the bulk values of the dielectric constant, indicates that the theoretical predictions for the parasitic inductance are of the correct order of magnitude.

9.3 Comparison of the measured data with other published results.

Published data on the measured properties of microwave capacitors at X band are extremely limited. In addition, the direct comparison of the published data can be irrelevant, due to the many interrelating factors which significantly affect the overall capacitor characteristics. Any meaningful comparison of results can therefore only be achieved after a thorough investigation of the capacitor fabrication processes involved, and the measurement techniques employed, for each of the capacitors under discussion.

Published results currently available are due to Caulton[98,145], Katoh[161] and Butlin[7], of which the latter is concerned only with the properties of the dielectric materials.

The first measurements to be performed were by Caulton [2] and these indicated that capacitor Q factors of between 40 and 60 could be achieved at 2 GHz, using silicon dioxide deposited from silane as the dielectric.

It was appreciated [174], however, that the silicon dioxide thus obtained included trapped water vapour, and in addition, was extremely porous. This then allowed the atoms to move in an r.f. field and resulted in large loss factors. However, by heating the dielectric at between 450°C and 1000°C, the oxides could be densified, and the trapped water vapour driven off. From infra-red, and p etch rate investigations on the densified dielectrics [174], it was shown that the resulting dielectric properties approached those of bulk quartz. This then suggested that values of dielectric Q factor for densified silicon dioxide could feasibly be close to the value of 10,000 for bulk quartz.

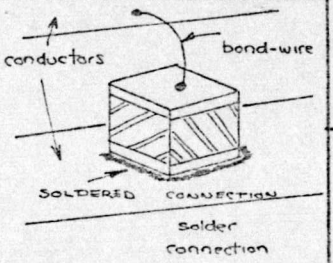
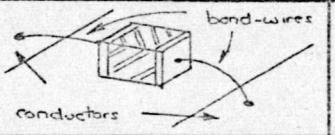
Caulton, therefore, concentrated his measurements on densified dielectrics, and his later results [98] showed a reduction in the capacitor loss, but the capacitor Q factors were still limited to around 100 at 2 GHz. This, therefore, was taken to indicate that the electrodes were the most significant factor in the capacitor loss.

At a later date, Caulton [145] extended his measurements to the 8 - 12 GHz region, and the results, summarised in figure 9.3, confirm his earlier findings at 2 GHz, that the electrode loss is the main source of capacitor loss.

Caulton's measured values of capacitor Q factor are of the same order of magnitude as those obtained by the author (figure 9.3), but there is total disagreement as to the main source of capacitor loss, with Caulton promoting the electrode loss, and the author promoting the dielectric loss.

The method of calculation of the capacitor properties is fundamentally the same in both measurement techniques, in so far as the capacitor properties are calculated by "subtracting out" the effects of the interconnections between the capacitor and the measurement system. In Caulton's measurements, the interconnections are bond-wires, and their

Comparison of published data on microwave capacitors. Figure 9·3

DATA SOURCE	SAMPLE	DIELECTRIC MATERIAL	CAPACITOR DIMENSIONS L = LENGTH W = WIDTH T = THICKNESS	CAPACITOR CONFIGURATION	MEASURED CAPACITOR PROPERTIES AT 8·6 GHz						
					ELECTRODE MATERIAL SURFACE RESISTIVITY	CAPACITANCE pF.	CAPACITOR Q FACTOR	ELECTRODE Q FACTOR	DIELECTRIC Q FACTOR	DIELECTRIC CONSTANT ε_d	Bulk material DIELECTRIC CONSTANT
CAULTON (ref. 145)	A	SiO_2 highly densified	not available N/A		N/A	0·9	85	87	> 5000	N/A	3·78
	B	SiO_2 highly densified	N/A		N/A	3·6	30	31	> 5000	N/A	3·78
	C	SiO_2 less densified	N/A		N/A	0·75	200	300	600	N/A	3·78
KATOH (ref. 161)	D	SiO_2 not densified	L = 2·7mm W = 3·3mm T = 0·01mm	2D configuration (figure 6·6)	0·8 Ω/□	9·7	< 1	< 1	N/A	12·3	3·78
MICHIE	6	SiO_2 not densified	L = 240 W = 125 T = 1·1	3D configuration (figure 6·14)	0·07 Ω/□	0·9	137	1360	159	3·55	3·78
	7	SiO_2 not densified	L = 225 W = 142 T = 1·0		0·07 Ω/□	1·07	139	1800	160	3·50	3·78
	11	Al_2O_3 not densified	L = 213 W = 80 T = 1·2		0·07 Ω/□	1·26	189	1465	240	8·75	9·6 – 9·9

impedance is significantly larger than the impedance of the capacitor itself (the bond-wire reactance is up to 9 times the reactance of the measured capacitor, and the bond-wire loss is up to 4 times the capacitor loss). Significant errors in the calculated values of the capacitor properties will therefore result if errors exist in the assumed values of bond-wire impedance, and this in turn will lead to substantial errors in the calculated dielectric properties.

In contrast, in the author's measurements, the interconnections are short lengths of microstrip, and the impedance introduced due to the interconnections, is less than 10% of the capacitor impedance. The resulting error in the dielectric properties will therefore, in comparison, be substantially smaller than for Caulton's measurements.

It is therefore postulated that the higher electrode losses encountered by Caulton are due to bond-wire resistance for which he has not fully accounted. In addition, for the first two measured samples, Caulton states that he has not taken into consideration the resistance of the solder connection between the capacitor and the conductor (figure 9.3), which could account for the relatively low Q factor of these capacitors when compared to the third sample.

If these factors are, in fact, relevant, then the values of dielectric Q factor quoted by Caulton will be inflated, and the electrode Q factors will be underestimated.

It is acknowledged, however, that the Q factors of the dielectrics measured by Caulton will be higher than those measured by the author, as it has been shown[174] that the Q factors of silicon dioxide dielectrics obtained by r.f. sputtering, are lower than those obtained from silane deposition, with subsequent densification.

Katoh[161] presents results of one measurement on a thin film overlay capacitor, and this is presented in figure 9.3. His capacitor utilises the 2D configuration analysed in section 6.3, and it will be recalled from this section, that for high values of capacitance, to mininise the electrode inductance, and to achieve acceptable levels of electrode

Q factor, both the capacitor aspect ratio ($\frac{\text{width}}{\text{length}}$) and the dielectric constant of the capacitor dielectric material, must be extremely large. Katoh has ignored these important design rules, and for his 97 pF capacitor has utilised an aspect ratio of 1.2, with silicon dioxide as the dielectric. It is not surprising then, that the measured electrode Q factor is less than unity, and the value of dielectric constant predicted from the measured value of capacitance, which is inflated by any electrode inductance which is not accounted for, is 12.3 (bulk 3.78). His result is useful in so far as it serves to verify the major predictions outlined in section 6.3.

Butlin[7] has performed measurements of the dielectric constant and Q factor, of the dielectric materials in isolation, using cavity techniques. The major significance of Butlin's measurements is that they are performed on dielectrics which have been deposited from the same dielectric targets, using the same sputtering equipment and using nearly identical sputtering conditions, as the dielectrics deposited by the author, and measured using the capacitor measurement technique.

Therefore, if the properties of these dielectrics are measured using Butlin's cavity technique, and the author's capacitor technique, any difference encountered in the measured properties will then be due to experimental errors in the measurement systems, lack of reproducibility of the processing conditions, or any interaction between the capacitor electrodes and the dielectric, which affects the dielectric properties.

As was indicated previously, the dielectric deposition conditions have been varied for particular capacitors, to establish any relationship between the processing conditions and the resulting dielectric properties. The dielectric samples under investigation have therefore been divided into 3 distinct groups (i.e. in figure 9.4, groups X, Y and Z), and for samples within a particular group, the dielectric conditions are virtually identical, but between groups, they vary significantly.

COMPARISON OF THE MEASURED DIELECTRIC PROPERTIES USING THE CAPACITOR TECHNIQUE AND THE CAVITY TECHNIQUE[7]

FIGURE 9.4

GROUP	SUB-GROUP	DATA SOURCE	DIELECTRIC MATERIAL	SAMPLES (figures 9.1–9.2)	NUMBER OF SAMPLES	DEPOSITION CONDITIONS				MEASURED DIELECTRIC PROPERTIES x1, Y1, Z1 AT 8·6 GHz x2 Y2 Z2 AT 10.0 GHz	
						PRESSURE TORR	D.C. INPUT POWER WATTS	DEPOSITION RATE Å/min	FIELD Wb/m^2	DIELECTRIC Q	DIELECTRIC CONSTANT
X	X 1	MICHIE	SiO_2	1-3 5-9	8	1×10^{-3}	544	200	1·25	152 ± 12	3·58 ± 0·05
	X 2	BUTLIN[7]	SiO_2	–	2	1×10^{-3}	550	220	1·25	174 ± 30	3·62 ± 0·05
Y	Y 1	MICHIE	SiO_2	4 10	2	1×10^{-3}	475	135	–	168 ± 6	3·62 ± 0·08
	Y 2	BUTLIN[7]	SiO_2	–	2	1×10^{-3}	400	73	–	253 ± 3	3·55 ± 0·025
Z	Z 1	MICHIE	Al_2O_3	11 12	2	1×10^{-3}	720	185	1·25	218 ± 22	8·86 ± 0·1
	Z 2	BUTLIN[7]	Al_2O_3	–	1	1×10^{-3}	550	118	1·25	400	9·5

Within each of these groups are two sub-groups (suffix 1, suffix 2) which represent the samples measured by either the capacitor measurement technique (suffix 1), or the cavity measurement technique (suffix 2). Within each of these sub-groups, the processing conditions are nominally identical, but between the sub-groups, within a particular group, the conditions vary to a small extent, as indicated in figure 9.4.

From this figure, therefore, the effects of the processing variations on the properties of the dielectrics can be established by comparing samples in different groups (X,Y or Z), and the lack of processing reproducibility, inaccuracies in the measurement techniques, and interactions between the electrodes and the dielectric, can be investigated by comparing the samples in different sub-groups, but within the same group.

The results of the measured dielectric properties (figure 9.4) indicate that for the samples of group X, in which the sub-group processing conditions are, to all intents and purposes, identical, the dielectric Q factor and the dielectric constant measured using the two techniques, agree to within the accuracies of the techniques. The cavity technique suggests Q factors 12% higher, and dielectric constants 2.2% lower, than those predicted by the capacitor measurement technique.

This therefore verifies the basic accuracy of the capacitor measurement technique, and in turn, implies that the values of electrode Q factor, and parasitic inductance suggested in figure 9.2, are of the correct order of magnitude. This then augments the conclusion stated earlier, that the capacitor loss is determined primarily by the dielectric loss.

For the samples of group Y (in which the deposition rate in sub-group Y1 is approximately double the deposition rate of sub-group Y2) the results are less in agreement. However, comparing the results of sub-groups X1 - Y1 and X2 - Y2, the overall trend of the results is similar, in that for a reduction in the deposition rate, no trend is apparent for the measurement value of dielectric constant as they lie within the accuracies of the measurement techniques.

This trend is also confirmed within the sub-groups of group Y.

For the samples of group Z, in which the deposition rate of sub-group Z1 is greater than that of sub-group Z2, the same trend is displayed by the Q factor, but is reversed in the case of the dielectric constant. This latter factor is reduced in significance however, when it is considered that the difference in the measured values of dielectric constant is 0.4%, which is well within the accuracies of the measurement techniques.

Therefore, in summary, for nominally identical processing conditions, the dielectric properties predicted from the capacitor measurements agree well with those predicted from the cavity measurements. The processing conditions, however, significantly affect the dielectric properties, and in particular, a decrease in the dielectric deposition rate results in an increase in the Q factor and a decrease in the dielectric constant.

The results of both measurement techniques indicate that the Q factor of alumina is greater than that of silicon dioxide.

10. PROJECT CONCLUSIONS.

10.1 Major project conclusions.

The most important conclusions to be drawn from this project are

1) microwave overlay capacitors can be produced at 10 GHz with useful values of capacitance and Q factor, and the capacitors remain lumped throughout X band.

2) the properties of microwave overlay capacitors can be accurately measured using the resonator technique described in this thesis. Values of the dielectric Q factor and the dielectric constant measured using this technique, have been shown to be in good agreement with measurements on the dielectrics in isolation performed by Butlin[7], using cavity techniques.

10.2 Advantages and disadvantages of the resonator measurement technique for microwave overlay capacitors.

The advantages of the resonator technique are

1) the capacitors are measured in situ. The bond wires (which are a feature of other techniques), are not, therefore, required, and are replaced by microstrip feeders, which are, by comparison, very much smaller. This considerably reduces the parasitic inductance and resistance, and results in a significant increase in the accuracy of measurement of the capacitor characteristics.

2) in contrast to other techniques, connections to the capacitor electrodes are, geometrically, well-defined, and a realistic estimation of their inductance and resistance can therefore be achieved, resulting in a further increase in the accuracy of measurement of the capacitor characteristics.

3) since the equivalent circuit approach to the calculation of the capacitor properties is used. and not the perturbation technique, very large changes in frequency and Q factor can be permitted during the measurements, and this allows very accurate measurements to be obtained. The accuracy is, however, limited to the accuracy of the equivalent circuit model.

4) the accuracy of measurement of the effective capacitance is $\pm$ 1.025%, and of the effective capacitor Q factor is $\pm$ 7.2%.

The major disadvantage of the measurement technique is that a new test resonant line must be fabricated for each capacitor to be measured.

In addition to this disadvantage, there are several factors which, fundamentally, are second order effects, but nevertheless, limit the accuracy of measurement of the dielectric Q factor and the dielectric constant. It is anticipated that by further investigation, realistic estimates of these particular effects can be obtained, and the accuracy of measurement of the capacitor characteristics improved as a result.

These factors are

1) the theoretical estimations of the electrode and electrode feeder inductance and resistance have been assumed without conclusive verification of their accuracy.

2) the effects of skin effect on the current distributions in the microstrip line, the microstrip feeders, and the capacitor electrodes, have, to a large extent, been ignored.

3) the fringing capacitance associated with the test capacitor has been ignored.

10.3 Typical measured properties of microwave overlay capacitors.

For 1 pF capacitors, of the 3D configuration (figure 6.14), with aspect ratios (capacitor width/capacitor length) of between 1.6 and 3, using undensified r.f. sputtered silicon dioxide and alumina dielectric materials, measurements at 8.6 GHz have indicated that

1) the capacitor Q factor is determined predominantly by the dielectric Q factor.

2) dielectric Q factors of approximately 175 can be achieved using silicon dioxide dielectric materials.

3) dielectric Q factors of approximately 240 can be achieved using alumina dielectric materials (section 10.5)

4) dielectric Q factors can be improved by careful selection of the dielectric deposition conditions.

5) electrode Q factors of approximately 2500 can be achieved using copper electrodes.

6) for the frequency range 8 - 12 GHz, the variation of capacitance with frequency can be maintained to approximately 5.5% with relative ease.

10.4 Design criteria to improve overlay capacitor performance.

It has been shown

1) for capacitors with aspect ratios less than, or equal to, 5, significant improvements in the electrode Q factor, and significant reductions in the parasitic inductance, can be achieved by using the 3D capacitor configuration of figure 6.14 in preference to the 2D capacitor configuration of figure 6.6.

2) the capacitor aspect ratio is vitally important in achieving acceptable electrode Q factors, and in maintaining tolerable values of electrode inductance.

3) copper offers significant advantages as an electrode material in general, and in particular as the lower electrode material, when compared with other, lower conductivity materials.

4) the optimum thickness for the top electrode is 1.57 skin depths.

5) the optimum thickness for the lower electrode is 1 skin depth.

6) the minimum practical dielectric thickness is 0.5 μm for silicon dioxide, and 2 μm for alumina (section 10.5).

7) for the 2 D capacitor configuration, the upper practical limit of capacitance at 10 GHz, is 2.5 pF using silicon dioxide as dielectric, and is 4 pF using alumina as dielectric, due to the parasitic inductance. This is excluding any limitations introduced by the feeders.

Significantly higher values of capacitance can only be achieved by using high quality, high dielectric constant materials for the capacitor dielectric,

8) the microstrip feeder impedance can be extremely significant in relation to the capacitor impedance, and will be detrimental to the effective capacitor properties. The feeder lengths should therefore be kept to the absolute minimum, and the characteristic impedance kept as low as possible.

9) to avoid a weakness in the dielectric at the overlay of the lower electrode, the lower electrode should have a tapered edge profile.

10.5 Processing yields.

1) Processing yields for silicon dioxide capacitors were approximately 75%, which was considered a tolerable yield, and sufficiently high to justify the use of silicon dioxide as a dielectric in microwave capacitors.

The major factors affecting the yield, are, in approximate order of importance

a) environmental cleanliness

b) lower electrode edge profile.

2) Processing yields for alumina capacitors were approximately 5%, which was considered completely unacceptable for overlay capacitor production. The usefulness of alumina as a overlay capacitor dielectric will, therefore, be considerably limited unless significant improvements in the yield can be achieved.

The major factors affecting the yield, are, in approximate order of importance

a) quality of the dielectric target

b) environmental cleanliness

c) lower electrode edge profile.

10.6 Suggestions for further work.

The total number of microwave overlay capacitors measured in the course of this project, has been severely limited due to restrictions on the available time, and the measurements which have been performed, have only been sufficient

a) to indicate the capabilities of the measurement technique for the evaluation of the capacitor properties

b) to demonstrate that overlay capacitors can be fabricated with useful properties at X band.

There is, therefore, unlimited scope for the further development of overlay capacitors, and the measurement of their properties using the techniques described in this thesis. In particular, topics of immediate interest are

1) the determination of rigorous theories to describe the parasitics of the test capacitor in its measurement environment.

2) the further investigation of alumina as a dielectric material, with particular emphasis placed on improving the processing yield.

3) the investigation of the effects of densification on the dielectric properties.

4) the measurement of the dielectric breakdown voltage, and its correlation with the dielectric deposition conditions, the dielectric thickness, the lower electrode thickness, and the lower electrode edge profile.

In addition to these short-term investigations, there are listed below, three long-term projects which, it is envisaged, will yield extremely useful results.

1) It was anticipated at the outset of this project that the capacitor measurement technique would be used in conjunction with the computer correction facilities of Shurmer[151], already available at Warwick University. Due to limitations of time, it was impossible for this to be achieved in this particular project. However, should the two facilities be mated in the future, it is envisaged that a capacitor measurement technique of formidable capabilities will be obtained.

2) A section of the work described in this thesis which provided extremely valuable results for the minimum of outlay, was the measurement of the properties of capacitor electrodes using scaled model measurement techniques.

With the larger computer facilities recently made available at the Midland Regional Computing Centre, at Manchester University, computer simulation techniques could be applied to the analysis of these models (as has already been attempted on a small scale in Chapter 6), and the effects of variations in the electrode parameters on the overall capacitor characteristics, could then be rapidly assessed. The design of overlay capacitor electrodes could then be readily optimised.

3) In conjunction with the work currently being undertaken at Warwick University by Da Silva[175] on the design and construction of lumped-element microwave inductors, there is considerable scope for extending the research into the design and fabrication of complete microwave circuits.

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12.1

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SIMPLE RESONATOR METHOD FOR MEASURING DISPERSION OF MICROSTRIP

Indexing terms: Microwave measurements, Striplines, Permittivity measurement

The method uses the resonant frequencies of a simple straight microstrip resonator, short-circuited at both ends. It is excited by passing a current through one of the short circuits. Graphs of effective relative permittivity against frequency are given for resonators on alumina and quartz substrates, with an error of within only ±0·1%.

This letter presents a simple and practical microwave measuring technique, utilising a resonant line to determine the effective relative permittivity ε_{eff} of microstrip. Published works[1-7] in this field have shown that ε_{eff} increases with an increase in frequency, i.e. the line is dispersive. Hence the characteristic impedance of the line decreases with an increase in frequency. Therefore the variation of ε_{eff} with frequency should be known.

There are four methods of measuring ε_{eff} in common use:

(*a*) open-circuited resonant microstrip line[1]

(*b*) ring resonator[2, 3, 6]

(*c*) variation of phase of a line with frequency[3]

(*d*) nodal shift technique.[4]

Method *a* needs correction for the 'end effect', method *b* becomes difficult for wide strips of the microstrip line, method *c* requires correction for transition to the measuring equipment, and method *d* is very laborious. A comparison of these techniques[5] concluded that method *b*, the ring resonator, has been shown[6] to have a number of difficulties that require the use of a large substrate area to overcome. The new method presented overcomes these disadvantages.

Cooke[7] recognised that the short-circuit termination of a microstrip line could eliminate end effects. The method presented here uses a straight resonator with a short circuit at both ends. This configuration has resonant frequencies whenever the line length becomes a multiple of half a wavelength at that frequency.

The effective relative permittivity ε_{eff} for a microstrip line is defined such that

$$v = \frac{c}{\sqrt{\varepsilon_{eff}}}$$

where ε_{eff} is a function of frequency and the parameters of

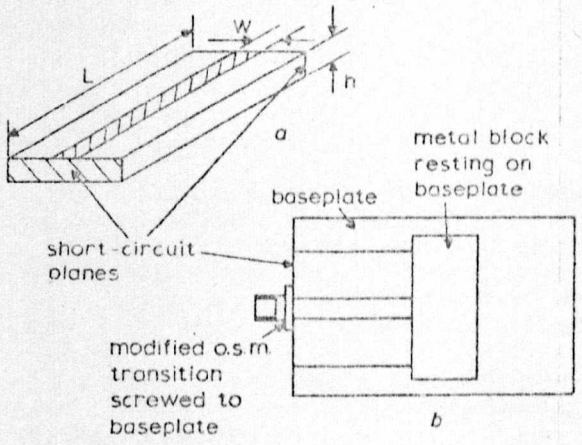

Fig. 1 *Microstrip resonator short circuited at both ends*
a Resonant line
b Test jig

the microstrip, and c is the velocity of light in free space. For an air-dielectric line with no dispersion, the resonant frequency f_0 would be

$$f_0 = \frac{nc}{2L}$$

where n is the number of halfwavelengths and L is the length of the microstrip line.

Let f_{ox} be the resonant frequency of the microstrip resonator with dispersion. Then

$$f_{ox} = \frac{nv}{2L} = \frac{nc}{2L\sqrt{\varepsilon_{eff}}}$$

Therefore

$$\varepsilon_{eff} = \left(\frac{nc}{2Lf_{ox}}\right)^2$$

Knowing the harmonic number n and the resonant frequency f_{ox} of the resonant line, ε_{eff} can be calculated.

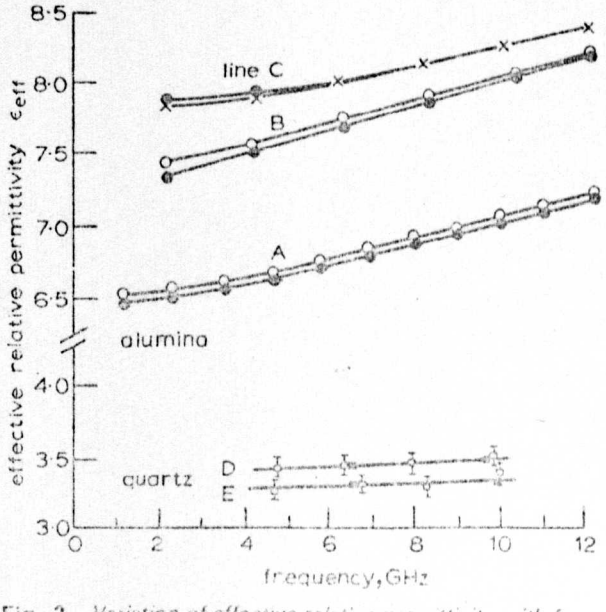

Fig. 2 *Variation of effective relative permittivity with frequency*
● ● ● with short-circuit block
○ ○ ○ without short-circuit block
× × × with silver-paint short circuits
□ □ □ nodal-shift technique
■ ■ ■ resonant-line technique

Table 1

Resonant line	A	B	C	D	E
Substrate material	alumina	alumina	alumina	fused quartz	fused quartz
Line length, mm	50·55	25·33	25·34	25·165	24·783
Strip width, mm	1·02	3·18	3·18	4·044	2·851
Substrate thickness, mm	1·02	1·02	0·635	0·489	0·499
Nominal impedance Z_0, Ω	50	26	20	18·5	24

Experimental work: Measurements of ε_{eff} against frequency were made in order to study the accuracy of this method. In particular, we examined the repeatability of the results and the effect of fringing fields on the short-circuit plane and the effect of using silver paint to make the short circuits. We also compared our results with those obtained by the nodal-shift technique.[4]

Measurements were made on the five lines shown in Table 1.

Short-circuit planes extended on both ends on the strip over the complete width of the ground plane, as shown in Fig. 1*a*.

The resonant line was excited through a single probe. The probe consisted of an o.s.m. microstrip adaptor, with the tab filed down to 0·3 mm by 0·2 mm, screwed onto the baseplate. The resonator was placed on the base plate, with the probe in contact with the short circuit to feed a current through it (Fig. 1*b*). This gave a sensibly constant coupling over the complete frequency range plotted. Careful checks were made to ensure that the coupling did not affect the resonant frequency. The measurements were made using an ordinary swept-frequency reflectometer connected to the probe. The resonance was indicated by a sharp decrease in the reflection coefficient.

If measurements of a restricted frequency range only are required, it is possible to find the value of n as follows: A hand-held probe (e.g. a screwdriver) is moved along the strip while the resonance is observed. The maximum shift of frequency is observed at every voltage maximum.

It was found that there is some 'field spillover' at the far end of the short-circuit plane. This can be overcome by a metal block placed as in Fig. 1*b* to extend the short-circuit plane to the fringing fields. At the probe end of the line, the body of the o.s.m. connector serves to extend the short circuit plane.

Fig. 2 shows some of the results obtained for ε_{eff} against frequency using this resonant-line technique. The variation of ε_{eff} for alumina substrates, with and without the metal block, is shown for lines A and B, and the effect of replacing the deposited short circuits with silver paint is shown for line C. For lines D and E, on quartz substrates, a comparison of results obtained by the resonant-line and nodal-shift techniques is shown. The latter gives a spread of ±2%, and excellent agreement between the two techniques was obtained. The expanded scale for ε_{eff} and the lack of scatter in the results are noteworthy.

It can be seen that failure to short-circuit the fringing fields can lead to errors of up to 1·4% for small n. The use of silver paint to form the short circuits does not affect the results too significantly. It does, however, lower the Q factor of the resonator and make the measurements much more difficult to perform.

The accuracy of this resonant-line method depends on the measurement of the length L of the line and the resonant frequency f_{ox}. L can readily be measured to a very high accuracy. Using a frequency counter, the accuracy of f_{ox} depends mainly on the Q factor of the resonator, typically 350. We have found that we can measure f_{ox} to an accuracy better than within ±0·1%. Thus, with care, a total accuracy of ε_{eff} of within ±0·1% can be achieved, and ±0·3% can be achieved with ease.

The method has advantages over other methods in its simplicity and accuracy, and it can be used on lines with wide strips where other methods become more difficult. For example, line D would require a 90 mm-square substrate to obtain accurate results using the ring-resonator method,[2, 6] whereas our results were obtained on a 25 mm-square substrate.

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PATENTS FORM NO. 3

12608

PATENTS ACT 1949

COMPLETE SPECIFICATION

5342/72
4th February, 1972

METHOD FOR DEPOSITING MATERIAL ON SELECTED AREAS OF A SURFACE

We, NATIONAL RESEARCH DEVELOPMENT CORPORATION, a British Corporation established by Statute, of Kingsgate House, 66 - 74 Victoria Street, London, S.W.1, do hereby declare the invention for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:-

The present invention relates to a method of forming a layer of a material in selected areas on a surface of the same or a different material, and to articles made by the method. The method is particularly but not exclusively useful in the fabrication of lumped components for microwave integrated circuits.

In such circuits components must be small compared to a wavelength, and for this reason a substrate with a low dielectric constant is chosen, for example quartz. The dielectric most commonly used in silicon dioxide SiO_2 because it is a low loss material. Obviously, as the dielectric and substrate are of the same material, etching of the dielectric will result in etching of the substrate thus preventing the dielectric area from being formed using conventional photolithographic techniques.

In low frequency circuit techniques, this problem can be overcome by depositing the dielectric through an out-of-contact metal mask which defines the dielectric area. For microwave integrated circuits, the required dielectric area is too small to be defined by a metal mask, the typical dimensions of a 1pF capacitor being 100 microns (μm) by 300μm. To deposit dielectric over an area of this size use can be made of a negative relief mask; that is a mask which forms a fairly thick covering in a shape which is the complement of the area of the required deposition.

If such a mask is made of photoresist any remaining particles of underdeveloped resist cause pinholes in the dielectric. This is, of course, disastrous in capacitor fabrication as a direct

short between electrodes results. It has also generally been found that the adhesion of films is impaired where photoresist once existed.

Alternatively, if such a mask is made of metal it can be made in two ways.

By depositing a thick layer of metal and then etching the required pattern. This results in severe undercutting of the metal, leading to poorly defined dielectric areas; or by depositing a thin layer of metal, etching the required pattern, and then plating to the required thickness. This virtually eliminates undercutting thus improving the area definition. However, plating up to the metal mask will also involve plating up of the connection to the lower electrode of a capacitor.

For these reasons, it can be seen that both photoresist relief masks and metal relief masks have severe disadvantages.

According to the present invention there is provided a method of depositing material in a selected area on a surface, including depositing a protective layer over, and in contact with, a surface which includes the area on which a material is to be deposited, the material of the protective layer having an etchant which does not attack the material or materials of the surface, depositing a layer of photoresist over the protective layer, exposing and developing the photoresist to provide a mask which is the complement of the said selected area, etching away that part of the protective layer revealed after developing the photoresist, depositing over that part of the said surface revealed after etching the protective

layer, a layer of that material, which it is required to deposition the selected area, removing the remaining photoresist, and etching away the remaining part of the protective layer.

The invention also extends to articles such as integrated circuits, thin film components, including thin film capacitors, made using the method of the preceding paragraph.

Since the material deposited on the selected areas is not etched, a material can be deposited in these areas on a surface of the same material, or a material can be deposited for which no suitable etchant exists. Since the photoresist is applied over the protective layer it is entirely removed in the selected areas before the material is deposited and no pinholes can form. Further, undercutting is avoided, as is plating up of the connection to the lower electrode in capacitor fabrication.

The material deposited adheres well to the surface since the photoresist has not been in contact with the surface, and there is no undercutting of the deposited material. In fact by varying the thickness of the protective layer deposit ed and varying the time for etching the parts of the protective layer away in forming the mask, the edge profile of the material deposited can be controlled. The method of achieving such control will be described in more detail later.

Additionally, since an out-of-contact mask is not used, definition is improved.

The protective layer may for example be copper, aluminium, chromium, gold or any material whose etchant does not attack the

photoresist or, in fabricating a capacitor a lower metal electrode which is deposited before the protective layer to form one electrode of the capacitor.

When making microwave capacitors suitable dielectric materials include Silicon Dioxide (SiO_2), Silicon Monoxide, Alumina (Al_2O_3), Yttrium Oxide, Silicon Nitride, and Tantalum Pentoxide (Ta_2O_5). Suitable substrates include Quartz (SiO_2), Alumina, Sapphire, ferrite and glass. The electrodes may for example be copper, gold, aluminium silver or tantalum.

When the electrodes are gold and the metal mask is copper the etchant for the copper may be Ferric Chloride.

The following photoresists may, for example, be used: Shipley positive types AZ 111, AZ 340, AZ 1350 or AZ 1350H; or Kodark negative types KPR, KRP 2, KPR 3, KMER, KOR and KTFR.

Certain embodiments of the invention will now be described by way of example with reference to the accompanying drawings, in which:-

Figures 1(a) and 1(b) are plan and cross-sectional views of the lower electrode of a thin film capacitor deposited on a substrate,

Figures 2(a) and 2(b) are plan and cross-sectional views after a metal layer has been deposited in making the capacitor using the method of the present invention,

Figures 3(a) and 3(b) are plan and cross-sectional views after photoresist has been applied to the copper layer and has been exposed and developed,

Figures 4(a) and 4(b) are plan and cross-sectional views after the metal layer has been etched away where revealed by the development of the photoresist,

Figures 5(a) and 5(b) are plan and cross-sectional views after a layer of dielectric has been deposited,

Figures 6(a) and 6(b) are plan and cross-sectional views after the remaining photoresist and copper has been removed,

Figures 7(a) and 7(b) are plan and cross-sectional views after the upper electrode of the capacitor has been deposited, and

Figures 8(a), 8(b), 9(a) and 9(b) are cross-sectional views illustrating how material can be deposited using the method according to the present invention to give a desired edge profile to the material deposited.

In the above mentioned figures the vertical scale is enlarged relative to the horizontal scale in order to show detail clearly.

In Figures 1(a) and 1(b) the lower gold electrode 10 of a capacitor to be fabricated has already been deposited on a quartz substrate 11 using a conventional photolithographic technique. Such techniques are described in "An Introduction to Photofabrication using Kodak Photosensitive Resists", Kodak publication No.P-79. The materials used are a chromium seed layer 500Å thick, and gold 0.5μm thick. The etches used are chromium: 50 grams potassium ferrocyanide, 15 grams sodium hydroxide and 200 cc water; and gold: solution of iodine in potassium iodide.

A protective layer 12 of copper one μm thick is then deposited by evaporation at 10^{-6} torr over the whole surface of the substrate 11

and the gold electrode 10, the result being as shown in Figures 2(a) and 2(b).

Next a layer of photoresist 13, typically 20μm thick but varying between 10 and 30μm depending on the thickness of silicon oxide to be deposited, and the area to be covered, is applied over the copper layer 12 by dip coating. After allowing the volatile solvents in the photoresist to evaporate by leaving for ten minutes, the substrate, gold electrode and photoresist are baked at 70°C for twenty minutes. The photoresist is then exposed for ten minutes through an optical mask and developed [see Figures 3(a) and 3(b)] for five minutes in Shipley AZ 303 developer, diluted one part to four parts water. The exposure is such that the part of the photoresist remaining after development is the complement or "negative" of the areas where the dielectric is to be deposited. A suitable photoresist is Shipley positive AZ 111. After development the remaining photoresist is baked at 70°C for thirty minutes. The copper is then etched away at room temperature where revealed through the development of the photoresist. This etch is carried out for ninety seconds and gives the negative relief mask of Figures 4(a) and 4(b). The etchant used is 0.05 gms of ferric chloride per cubic centimetre of water.

A one μm layer of silicon dioxide 14, the dielectric for the capacitor, is now deposited by sputtering at 5×10^{-3} torr in 99.995% pure Argon at 20°C to give the situation shown in Figures 5(a) and 5(b). Then the remaining photoresist is removed by soaking in acetone with gentle agitation, and the remaining copper

is etched away in ferric chloride with the result shown in Figures 6(a) and 6(b). Lastly another gold contact 15, 0.5μm thick, is deposited using a conventional photolithographic technique as mentioned in connection with electrode 10 [see Figures 7(a) and 7(b)]. The contact 15 and the unprotected area of lower electrode 10 are then electroplated to 3μm.

One further advantage of the above method is that some control over the edge profile of the material deposited is possible. For example if the copper layer is say 1μm thick and it is etched, as described above, prior to deposition of the dielectric for a comparatively short time, say 90 seconds, then only a small amount of undercutting occurs (see Figure 8(a)) and the edge profile as shown at 16 in Figure 8(b) is nearly vertical. For a longer etching time, say 120 seconds, then more undercutting occurs Figures 9(a) and 9(b) with the result that the edge profile 17 is inclined to the vertical. A dielectric edge profile as shown in Figure 9(b) substantially avoids the possibility of a discontinuity in the upper electrode at the point where it passes over an abrupt step at the edge of the dielectric layer.

WHAT WE CLAIM IS:-

1. A method of depositing material in a selected area on a surface, including depositing a protective layer over, and in contact with, a surface which includes the area on which a material is to be deposited, the material of the protective layer having an etchant which does not attack the material or materials of the surface, depositing a layer of photoresist over the protective layer, exposing and developing the photoresist to provide a mask which is the complement of the said selected area, etching away that part of the protective layer revealed after developing the photoresist, depositing over that part of the said surface revealed after etching the protective layer, a layer of that material, which it is required to deposit on the selected area, removing the remaining photoresist, and etching away the remaining part of the protective layer, the method being such that the material which it is required to deposit is deposited on the surface in the selected area only.

2. A method of depositing material in selected areas on a surface, including depositing a protective layer over a surface of a substrate which includes areas on which a material is to be deposited, the material of the protective layer having an etchant which does not attack the material or materials of the surface, depositing a layer of photoresist over the protective layer, exposing and developing the photoresist to provide a mask which is the complement of the said selected areas, etching away that part of the protective layer revealed after developing the photoresist, depositing, by other

than electrodeposition, over the photoresist mask and the revealed part of the surface, a layer of that material, which it is required to deposit on the selected areas, removing the remaining photoresist and etching away the remaining part of the protective layer, the method being such that the material which it is required to deposit is deposited on the surface in the said selected areas only.

3. A method of depositing electrically non-conducting material in a selected area on a surface, including depositing a protective layer over a surface which includes the area on which the electrically non-conducting material is to be deposited, the material of the protective layer having an etchant which does not attack the material or materials of the surface, depositing a layer of photoresist over the protective layer, exposing and developing the photoresist to provide a mask which is the complement of the said selected area, etching away that part of the protective layer revealed after developing the photoresist, depositing over that part of the said surface revealed after etching the protective layer, a layer of the electrically non-conducting material, removing the remaining photoresist, and etching away the remaining part of the protective layer, the method being such that the electrically non-conducting material is deposited on the surface in the said selected area only.

4. A method of making one or more capacitors according to any preceding claim wherein the material which is deposited on the said selected area or areas is a dielectric material, including forming a first electrode or electrodes by depositing an area or areas of conducting material within, or extending into, the selected area or

areas before the protective layer is deposited, and depositing another area or areas of the said conducting material or another conducting material over the dielectric material after the photoresist and the protective layer have been removed to form a second electrode or electrodes, the said conducting material being a different material from the material of the protective layer and one which is not etched by at least one etchant for the material of the protective layer.

5. A method according to any preceding claim wherein the protective layer includes at least one of the following: copper, aluminium, chromium, nichrome, nickel, and gold.

6. A method according to any preceding claim wherein the material which is deposited on the said selected area or areas includes at least one of the following: silicon dioxide, silicon monoxide, alumina, yttrium oxide, silicon nitride, and tantalum pentoxide.

7. A method according to any preceding claim wherein the material forming the said surface includes quartz or alumina, or sapphire, ferrite or glass.

8. A method according to Claim 5 or 6 or 7 insofar as dependent on Claim 4, wherein the, or one of the, conducting materials is copper, or gold, or aluminium, or silver or tantalum.

9. A method according to any preceding claim wherein the photoresist is of a type which requires hardening before part of the protective layer is etched away, including the step of baking the photoresist for a time and at a temperature sufficient to ensure it

is not wholly or partially removed when the said part of the protective layer is etched away.

10. A method according to any preceding claim wherein the etching away of that part of the protective layer revealed after developing the photoresist is carried out for a time determined by the required edge profile of the material which is to be deposited in the selected area or areas.

11. An article including a layer of material deposited in a selected area, or selected areas, of a surface by a method according to any preceding claim.

12. An integrated circuit including a layer of material deposited in a selected area, or selected areas, of a surface by a method according to any preceding claim.

13. An electrical thin-film component or a capacitor including a layer of material deposited in a selected area, or selected areas, of a surface by a method according to any preceding claim.

14. A method of depositing material in a selected area on a surface substantially as hereinbefore described with reference to Figures 1 to 7 of the accompanying drawings.

15. A method of depositing material in a selected area on a surface substantially as hereinbefore described with reference to Figures 1 to 7 and Figure 8 or Figure 9 of the accompanying drawings.

C. HASLER
Chartered Patent Agent
Agent for the Applicants

FIG. 1a.

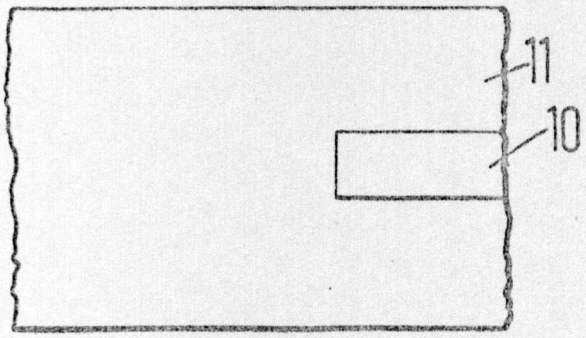


FIG. 1b.

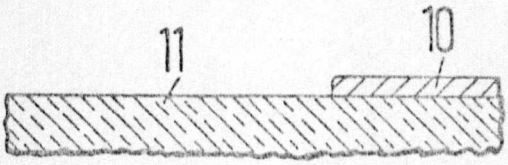


FIG. 2a.

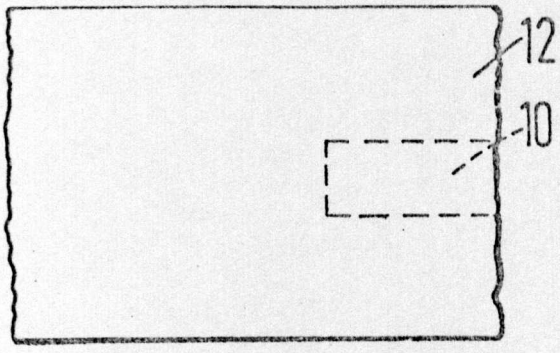


FIG. 2b.

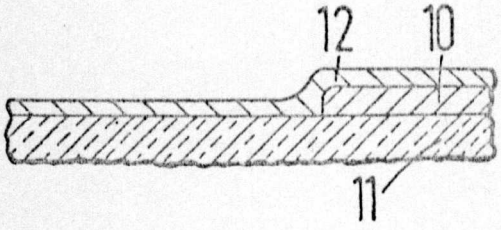


FIG. 3a.

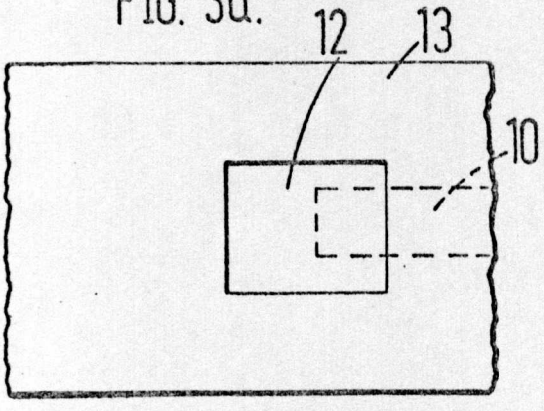


FIG. 3b.

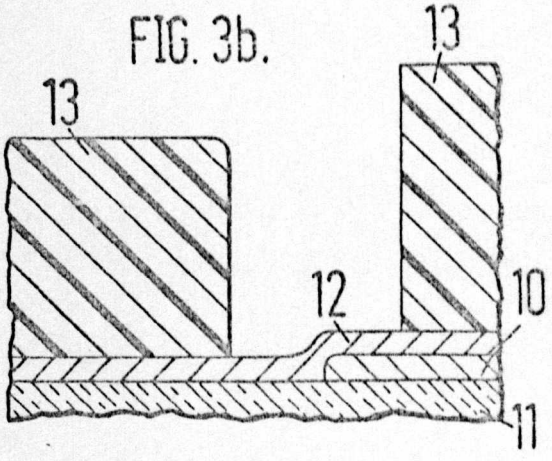


FIG. 4a.

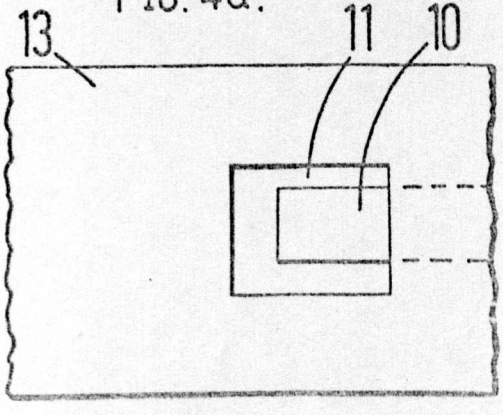


FIG. 4b.

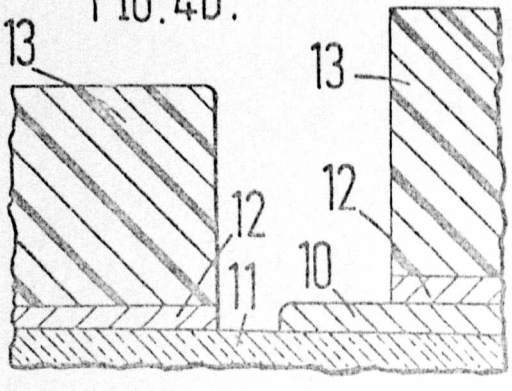


FIG. 5a.

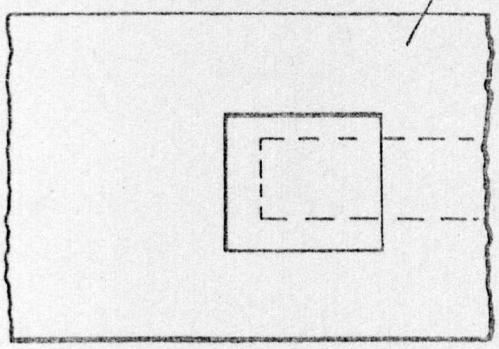


FIG. 5b.

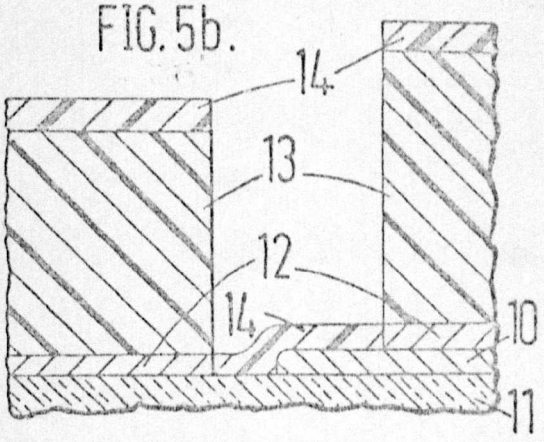


FIG. 6a.

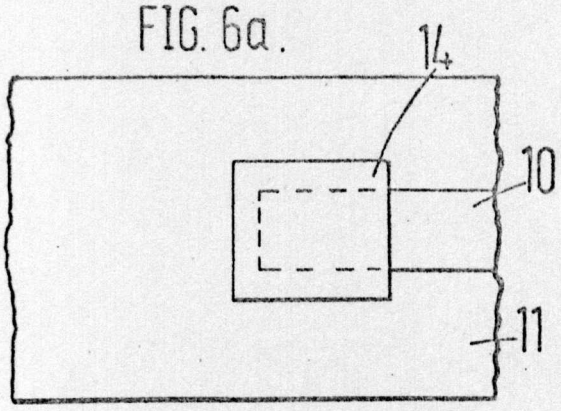


FIG 6b

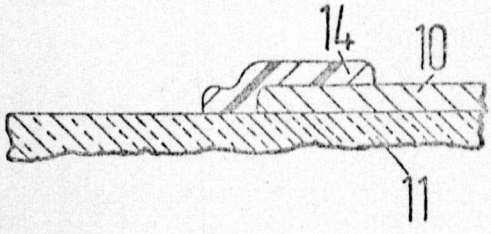


FIG. 7a.

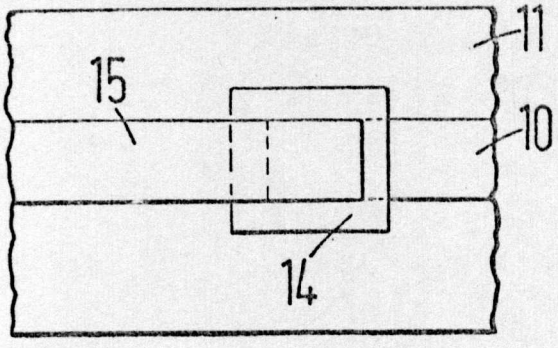


FIG. 7b.

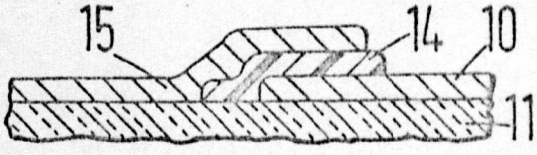


FIG. 8a.

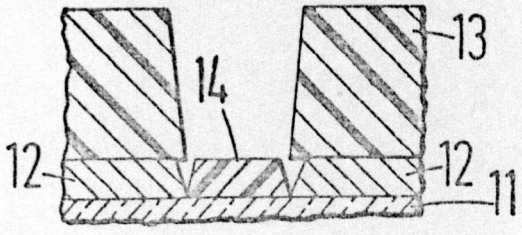


FIG. 8b.

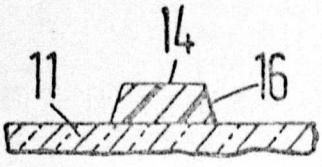


FIG. 9a.

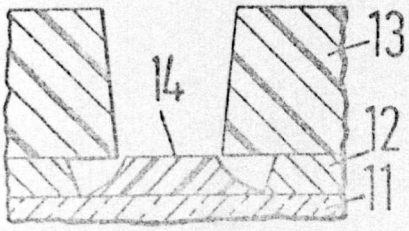
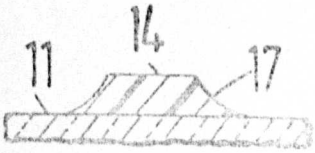


FIG. 9b.



12.3 Proceedings of the 1973 European Microwave Conference.
Vol.2 B.14.5.

MEASUREMENT OF OVERLAY CAPACITORS AT X-BAND WITH INDEPENDENT ASSESSMENT OF THIN-FILM CONDUCTOR LOSSES

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The accurate characterization of thin film microwave overlay capacitors has been impossible in the past, due to transition errors introduced by the enormous difference in size between the components and the measurement system. Most errors, particularly of loss, are due to the use of bond wires.

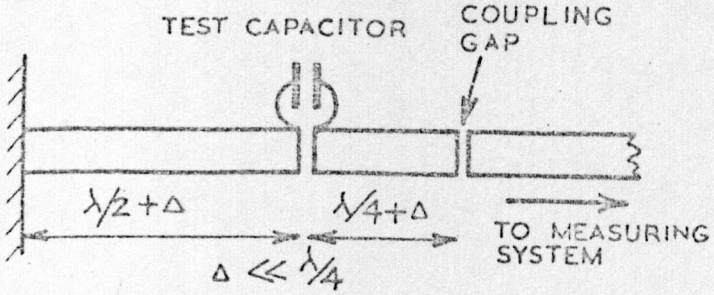
In this new technique the test capicitator is fabricated as an intrinsic part of an X-band microstrip resonator, eliminating the bond wires, and the capacitor can be measured in the same form as would be used in a practical circuit. Figs. 1 and 2 show the resonator. It is $3\lambda/4$ long with one end short circuited to the ground plane, and the other having a small gap coupling to the measurement system. The test capacitor is in series with the transmission line, positioned at a current maximum.

Conventional thin film techniques are used to construct the resonator. The test capacitor is constructed across a narrow gap in the resonator in two stages. At first it is made without a top electrode, and the resonant frequency and Q of the resonator plus capacitor are measured. Then the top electrode is completed and the measurements are repeated. The capacitor Q factor and capacitance are determined from these measurements and the physical dimensions of the resonator. The capacitance can be measured to within ± 1.2% and the Q factor to within ± 7%, using a resonator with an unloaded Q of 400, deposited on a quartz substrate.

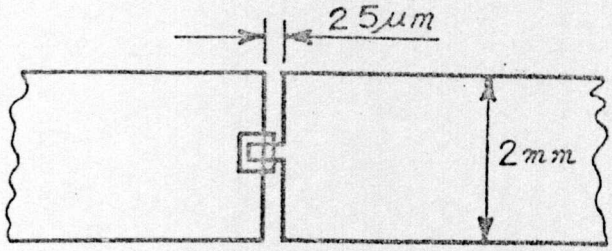
In Fig. 1c is shown a photograph of a completed 1 pF capacitor taken using a scanning electron microscope. Typically the lower electrode consists of 0.75 μm of evaporated copper, the dielectric is 1 μm thick SiO_2 deposited by R.F. sputtering, and the 5 μm thick copper upper electrode is first evaporated and then electroplated. A new photolithographic technique[1] was developed to make these capacitors.

The value of capacitance measured depends on two factors: the true capacitance and the electrode inductance. Similarly the Q factor depends on the electrode loss and the dielectric loss. Short electrodes, i.e. with width/length ratio $W/L > 4$, render the inductance negligible. To separate the contributions to the loss of the capacitor, independent measurements of dielectric loss[2] and electrode conductivity are needed. Here we report our measurements of electrode conductivity.

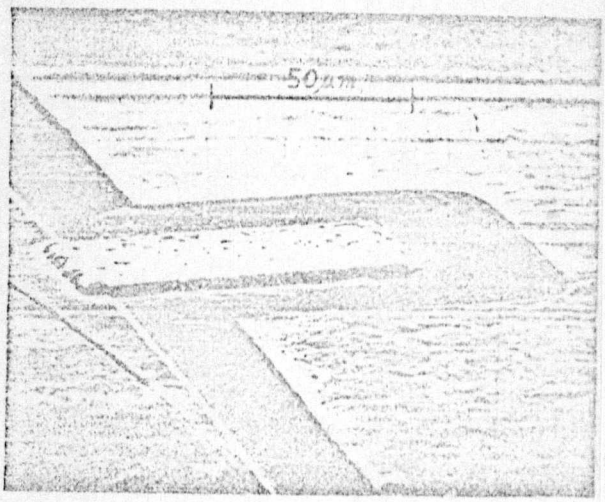
The Authors wish to thank the U.K. Science Research Council for financial support.



a). SCHEMATIC



b) CAPACITOR MOUNTED IN GAP



c) DETAIL OF CAPACITOR

FIG. 1. MICROSTRIP RESONATOR WITH OVERLAY CAPACITOR

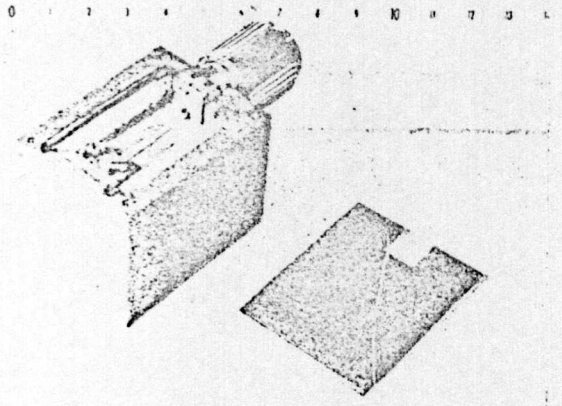


FIG. 2. MICROSTRIP RESONATOR MOUNTED IN SHIELDING BOX.

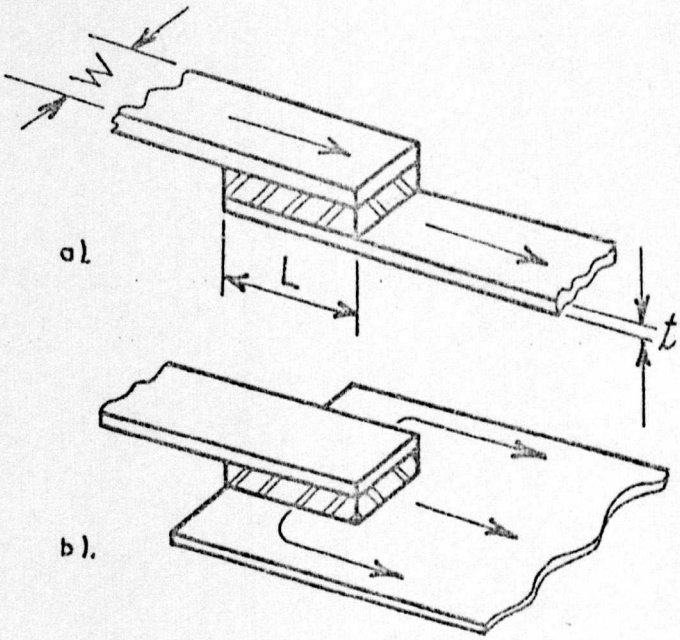


FIG. 3. TWO CAPACITOR CONFIGURATIONS (ARROWS INDICATE DIRECTIONS OF CURRENT FLOW.)

Dielectric	C(pF)	Q	Q electrode	Q dielectric	t(μm)	W/L
SiO_2	1.1	122	1557	133	1.1	1.6
SiO_2	1.0	120	1602	129	0.91	2.01
SiO_2	0,71	137	2349	145	0.72	3.0
Al_2O_3	1.25	164	1803	178	1.1	2.67

TABLE 2 Measurements on Capacitors at 9.5 GHz

TABLE 1 Measurements on metal films at d.c. amd 10 GHz

Deposition Method	Thickness (μm)	Surface resistance (ohms)		Microwave Conductivity $(\Omega m)^{-1}$		DC Conductivity $(\Omega m)^{-1}$		CLA (μm)	Theoretical DC Conductivity $(\Omega m)^{-1}$	Measured/Theoretical DC Conductivity (%)		Measured/Theoretical Microwave Conductivity (%)	
			annealed		annealed		annealed				annealed		annealed
		$\times 10^{-2}$	$\times 10^{-2}$	$\times 10^{6}$	$\times 10^{6}$	$\times 10^{6}$	$\times 10^{6}$		$\times 10^{6}$				
P.M.D. gold	5.1	3.38		34.5		36.9		0.07	41.0	90		84.1	
	4.6	3.38	3.28	34.5	36.6		40.4	0.07			98.6	84.1	89.3
Englehardt E56 gold	2.4	3.34		35.2		38.1		0.03	41.0	92.9		86.0	
	2.4	3.33		35.3		37.6		0.03	41.0	91.8		86.2	
Evaporated gold	2.5	3.48		32.5		34.8		0.02	41.0	84.9		79.3	
P.M.D. silver	3.3	3.03		43.3		47.8		0.05	62.9	76.0		68.9	
	3.3	3.00	2.91	43.7	46.5		52.0	0.07			82.6	69.5	73.9
Acid copper	3.5	2.98		44.2		49.7		0.05	58.0	84.6		76.2	
	3.5	2.99	2.96	44.0	44.9		50.5	0.04			87.1	75.9	77.5
Bright acid copper	3.2	2.91		46.6		52.7		0.03	58.0	90.8		80.4	
	3.2	2.90	2.84	46.8	48.8		53.0	0.03			91.3	80.7	84.2
Copper pyrophosphate													
Best result	4.5	2.89		47.1		47.2		0.03	58.0	81.4		81.2	
Worst result	4.8	3.05		42.3		45.4		0.04	58.0	78.4		73.0	
	4.8	3.05	3.03	42.3	42.9		46.0	0.04	58.0		78.3	73.0	73.9
Evaporated copper	3.1	2.86		48.1		52.1		0.01	58.0	89.9		82.9	

Experience shows that the surface resistance of the films used cannot be predicted from d.c. or l.f. measurements. A new cavity measurement technique[3] is used to measure the surface resistance in X-band. The sample metal film is deposited on a substrate and forms one end plate of an H_{011} cavity. Measurement of the return loss at resonance alone permits the sample surface resistance to be obtained directly from a graph. The maximum error in surface resistance is ± 0.0012 ohms.

Results one evaporated copper films[3] show that the microwave conductivity does not depend on film thickness, and the theoretical relation between film thickness and surface resistance is followed closely in practise. A series of factorially designed experiments[4] was made on films deposited from acid copper electroplating solutions. The effects of plating parameters were related to surface finish, surface resistance, and d.c. conductivity of the films. The composition of the plating solution was shown to be the most important factor.

Table 1 summarizes results obtained at 10 GHz from films deposited using evaporation and electroplating solutions. Two films were deposited from each solution and their microwave surface resistance measured; the d.c. conductivity of one of the films was then measured. The other film was annealed at 250°C for 2 hours in vacuum, and its microwave surface resistance and d.c. conductivity then measured. The copper pyrophoshate solution initially gave the best result, but these solutions deteriorate rapidly, and this result could not be repeated.

We conclude that lowest surface resistance is obtained from acid copper solutions with added brightener, and the effect of annealing on these films is small. Measured microwave conductivities are between 89% and 94% of the measured d.c. values, an effect we attribute to impurities in the film, not surface roughness. Use of silver plating is not advised. Annealing of plated gold films is required to achieve low loss.

Some results of measurements on capacitors are shown in table 2.

We conclude that for these dielectrics, the dielectric loss predominates for capacitors with values smaller than 10 pF, the electrode loss becoming significant for C > 10 pF. The electrode loss is dominated by the lower electrode whose thickness is limited by the need for the dielectric to overlap it. Decreasing the lower electrode thickness below 0.75δ (δ=skin depth) gives a rapidly increasing loss. If the upper electrode thickness exceeds 3δ, its contribution to the electrode loss is negligible. The electrode Q factor can be greatly increased by using the configuration of Fig. 3b rather than Fig. 3a. This results in an increase of electrode Q of 75% for W/L = 1.

We expect R.F. sputtered alumina to give much higher dielectric Q factors when the deposition process is optimized.

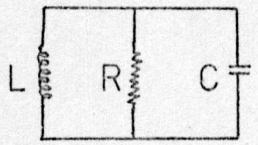
References

1. R.S. Butlin and D.F. Michie "Method for depositing material on selected areas of a surface" U.K. Patent Application 5342/72.
2. M.K. McPhun and K. Mehmet "Thin film dielectric measurements" chapter of "High frequency dielectric measurements" IPC Science and Technology Press 1973.
3. R.S. Butlin and M.K. McPhun "Surface-resistance measurements of thin conducting films at 10 GHz" Electronics Letters 8, 26, p 637-639, 28th Dec. 1972.
4. O.L. Davis "Design and analysis of industrial experiments" Oliver and Boyd, 1954.

APPENDIX 1.1

Derivation of the expression $\left(\frac{\Delta f_{DE}}{\Delta f_{LE}}\right)^3$

Consider the circuit diagram of figure A.1.1.1.



lumped resonant circuit

figure A.1.1.1.

If Q_{LE} = Q factor of the Lumped circuit

$$= \omega C R$$

$$= \frac{R}{\omega L}$$

Consider the circuit diagram of figure A.1.1.2 in which the lumped capacitor has been replaced by a distributed capacitance.

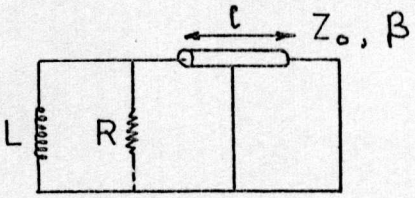


figure A.1.1.2.

$$Y = \frac{1}{R} + \frac{1}{j\omega L} + \frac{j}{Z_o} \tan \beta l \qquad \text{A.1.1.1}$$

If Q_{DE} = Q factor of the distributed circuit

$$= \frac{1}{2} \frac{\omega_o}{G} \frac{d\beta}{d\omega}\Bigg|_{\omega = \omega_o}$$

i.e. $$Q_{DE} = \frac{\omega}{2} R \left[\frac{l}{v} \frac{\sec^2 \beta l}{Z_o} + \frac{1}{\omega^2 L} \right]_{\omega = \omega_o}$$

At resonance, from equation A.1.1.1

$$\tan \beta_o l = \frac{Z_o}{\omega_o L} \qquad \text{A.1.1.2}$$

Therefore $$Q_{DE} = \frac{\omega R}{2}\left[\frac{l}{v}\frac{\sec^2 \beta l}{Z_o} + \frac{1}{\omega^2 L}\right]_{\omega=\omega_o}$$

$$Q_{DE} = \frac{Q_{LE}}{2}\left[1 + \beta l \frac{\sec^2 \beta l}{\tan \beta l}\right]_{\omega=\omega_o}$$

$$Q_{LE} = \frac{2 Q_{DE}}{1 + \frac{2 \beta l}{\sin 2 \beta l}}$$

But from equation A.1.1.2.

$$\beta l = \arctan \frac{Z_o}{\omega_o L} = \arctan \omega_o C Z_o$$

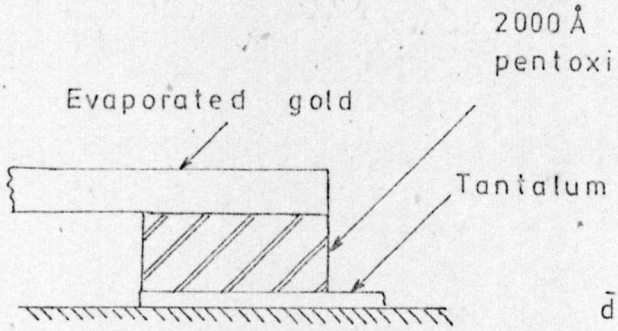
$$Q_{LE} = \frac{2 Q_{DE}}{1 + \frac{2 \arctan \omega_o C Z_o}{\sin 2 (\arctan \omega_o C Z_o)}}$$

Therefore $$\frac{Q_{LE}}{Q_{DE}} = \frac{2}{1 + \frac{2 \arctan \omega_o C Z_o}{\sin 2 (\arctan \omega_o C Z_o)}}$$

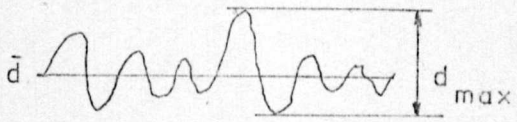
Since $Q \propto \frac{1}{\Delta f}$

$$\frac{\Delta f_{DE}}{\Delta f_{LE}} = \frac{2}{1 + \frac{2 \arctan \omega_o C Z_o}{\sin 2 (\arctan \omega_o C Z_o)}}$$

APPENDIX 1.2



Capacitor cross section



Talysurf trace

Substrate material	$\bar{d}$ Å	d_{max} Å	Cap. μF	DC leakage at $3{\cdot}75 \times 10^6$ V/cm	Yield %	85°C at working electric field — time of life (hours)
Soft glass sheet	300	1,000	0·035	0·005	100	7,600
96% Alumina (polished)	2,800	17,000	0·035	0·01	75	1,000
96% Alumina (as-fired)	12,500	40,000	0·042	0·06	25	0

The effect of substrate surface roughness on overlay capacitor properties[14]

APPENDIX 1.3

Derivation of the equation for the Q of a microstrip resonator.

Consider the shunt resonant circuit of figure A.1.3.1

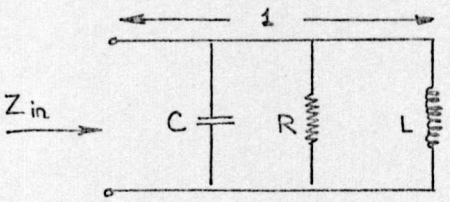


figure A.1.3.1

transmission coefficient

$$\gamma = \alpha + j\beta$$

The input impedance is $Z_{in} = Z_o \tanh \gamma l$

For low loss lines, as $\alpha l \to 0$ $\quad \sinh \alpha l \to \alpha l$

$\cosh \alpha l \to 1$

Therefore $Z_{in} \doteq Z_o (\alpha l \sec^2 \beta l + j \tan \beta l)$

i.e. $Y_{in} \doteq Y_o (\alpha l \operatorname{cosec}^2 \beta l - j \cot \beta l)$

$= G + jB$

At resonance $Q = \frac{1}{2} \frac{\omega_o}{G} \frac{dB}{d\omega} \Big|_{\omega = \omega_o}$

Therefore $Q = \frac{B}{2\alpha}$

where α is the line attenuation in Nepers/metre

$= \alpha_c + \alpha_d$

where α_c is the conductor attenuation

α_d is the dielectric attenuation

Conductor attenuation

At resonance, the real part of the input impedance is

$$R = Z_o \alpha l \sec^2 \beta l \Big|_{\omega = \omega_o}$$

For resonance $\beta l = \frac{\pi}{2}$

Therefore $R = Z_o \alpha l$

therefore $\alpha_c = \frac{R}{Z_o}$ nepers/metre

Assuming that the current distribution is uniform and equal to $\frac{I}{W}$ in both conductors, where I is the total current and W is the width of the microstrip line, and that the current is confined to the region $|x| < \frac{W}{2}$, and assuming the conductor and ground plane conductivities are equal, then

$$R = \frac{R'_s}{W}$$

where R'_s is the surface resistivity in $\Omega/\square$, assuming field penetration to 1 skin depth.

Therefore $\alpha_c = \frac{R'_s}{Z_o W}$ nepers/metre 20

But $R'_s = (\pi f \mu \rho)^{\frac{1}{2}}$

where f is the frequency

$\mu = \mu_o \mu_r$ is the permeability

ρ is the resistivity of the conductor

Therefore $\alpha_c = \frac{(\pi f \mu \rho)^{\frac{1}{2}}}{Z_o W}$

For a 32 ohm line in quartz, with copper plate of conductivity 47×10^6 mhos/metre at 10 GHz, $\alpha_c = 0.44$ nepers/metre.

Dielectric attenuation

As a major part of the electric field is confined to the substrate, a simplification can be made by assuming a plane wave in the dielectric, and the attenuation constant α_d is given by equation 1.2

$$\alpha_d = \tfrac{1}{2} \frac{\omega}{v} \tan \delta$$

For quartz, with $\tan\delta \doteqdot 2 \times 10^{-4}$ at 10 GHz,

$$\alpha_d \doteqdot 0.034 \text{ nepers/metre}$$

which is an order of magnitude lower than the conductor loss. To a first approximation, we shall ignore the substrate loss so that

$$Q \doteqdot \frac{\beta}{2\alpha_c} \quad \text{where } \beta \text{ is the phase constant}$$

$$Q \doteqdot \frac{\beta Z_o W}{2(\pi f \mu \rho)^{1/2}}$$

which can be reduced to

$$\underline{Q \doteqdot \tfrac{1}{6} W\sqrt{E_{eff}}\ Z_o\sqrt{F_{GHz}\,\sigma}}$$

where W is the strip width in metres.

E_{eff} is the line effective dielectric constant.

Z_o is the line impedance.

F is the resonant frequency in GHz.

σ is the conductivity in mhos/metre.

APPENDIX 2.1

Chemical analysis of deionised water as obtained using the Elgastat B106 deionising column.

	STANDARD TAP WATER	DEIONISED WATER
pH	5·50	5·00
Chloride (as Na Cl)	96·0 p.p.m.	32 p.p.m.
Sulphate	not present	not present
Hardness	180 ppm	not present
Permanent hardness	not present	not present
Alkalinity to phenolpthalein	not present	not present
Alkalinity to methyl orange (as $NaHCO_3$)	195 p.p.m.	18 p.p.m.

APPENDIX 2.2

Vacuum evaporation and glow-cleaning.

After insertion of the test samples in the vacuum unit, the normal pumping cycle is commenced, and the pressure allowed to fall to approximately 1×10^{-5} Torr. Once this pressure is attained, the baffle valve is closed slightly to reduce the pumping speed of the diffusion pump, and air is bled into the chamber through a needle valve. The H.T. voltage is applied to obtain a discharge, and the needle valve and H.T. adjusted for an H.T. voltage of 1 kV, and an H.T. current of 100mA. This provides a sufficiently strong discharge to clean the substrates.

After the shutter is opened, each side of the substrate is cleaned for 5 minutes, after which the H.T. is cut off, the needle valve closed, and the baffle valve opened to allow the diffusion pump to pump at its full rate.

After 30 minutes, the evaporation can be performed using the conditions given in Appendix 2.3.

After the evaporation, the unit is allowed to pump down for at least 30 minutes before removal of the substrates, to prevent excessive oxidation of the films.

APPENDIX 2·3

Vacuum evaporation and R.F sputtering conditions

VACUUM EVAPORATION CONDITIONS					
Pressure : 1×10^{-5} Torr Source – substrate distance : 4·5 inches					
METAL	H.T. VOLTAGE kV	H.T. CURRENT mA	filament current A	deposition rate Å/minute	CRUCIBLE
Chromium	2	7·5	24	180	ceramic
Copper	3·5	65	25	960	ceramic
Gold	3·5	60	25	1800	molybdenum

RF SPUTTERING CONDITIONS					
Pressure : 1×10^{-3} Torr Source – substrate distance : 3·9 cms Atmosphere : argon					
MATERIAL	H.T. VOLTAGE kV	H.T. CURRENT mA	D.C. INPUT POWER watts	FIELD Wb/m^2	DEPOSITION RATE Å/minute
silicon dioxide	1·7	320	544	1·25	200
alumina	1·8	400	720	1·25	165

Appendix 2.4

Metal Etchants

MATERIAL		ETCHANT	Approximate etch rate
Gold		32 grams Potassium Iodide 8 grams Iodine 200 ml water	1 μm/minute
Copper	1	10 grams ferric chloride 200 ml water	0·5 μm/minute
	2	200 grams chromium trioxide 5cc conc. H_2SO_4 (s.g. 1·84) 200 ml water	0·65 μm/minute
Chromium		40 grams potassium ferricyanide 12 grams sodium hydroxide 200 ml water (to be made immediately prior to use)	0·075 μm/minute

Plating Conditions

PLATING SOLUTION	BRIGHT COPPER SULPHATE	P.M.D. GOLD TRANSTHERM	EL 221 ELECTROLESS GOLD
constituents	175gms $CuSO_4$ 30cc conc. H_2SO_4 (s.g. 1·84) 0·01grams $CuCl_2$ 0·3 cc Cuprostar 914 15cc Cuprostar 701 4·6cc Cuprostar AA2 1 litre D.I. water	commercial	commercial
anode	copper	gold	none
anode area	15 cm^2	9 cm^2	—
electrode separation	30 cms	8·9 cms	—
voltage	1·5 volts	2·0 volts	—
current density	25·4 mA/cm^2	1·45 mA/cm^2	—
bath temperature	20° C	65° C	75° C
agitation	air	magnetic stirrer	magnetic stirrer
plating rate	0·48 μm/minute	0·088 μm/minute	0·03 μm/minute

APPENDIX 3.1

Fabrication of test samples.

The test samples used for the measurements in Chapter 3, were deposited on 1" x 1" x 0.020" fused quartz substrates, and consisted of copper conductors, 5 μm thick, and protected by 0.1 μm of gold.

The processes used, which evolved as the optimum, are described below, with references, as required, to the text of Chapter 2.

Substrate preparation

Polish substrate edges to remove bevel

↓

Clean substrates Section 2.4.2

↓

Glow-clean substrates Appendix 2.2

↓

Evaporate 200 Å chromium, 0.25 μm of copper over two large substrate faces and two edges. Appendix 2.3

↓

Apply 2.5 μm thick layer of K.T.F.R. resist Section 2.4.7

↓

Expose and develop Section 2.4.7

↓

Clean reverse face of substrate, and the edges, with trichloroethylene, acetone, I.P.A., Neutra clean 68. Wash thoroughly in water and spin dry.

↓

Touch-up photoresist as required, with Lacomit.

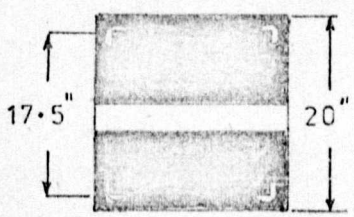
↓

Electroplate, using bright copper plate. Section 2.4.11

↓

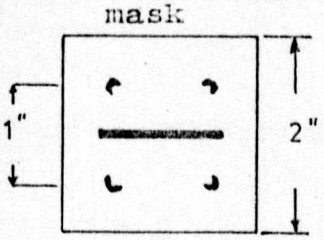
Mask preparation

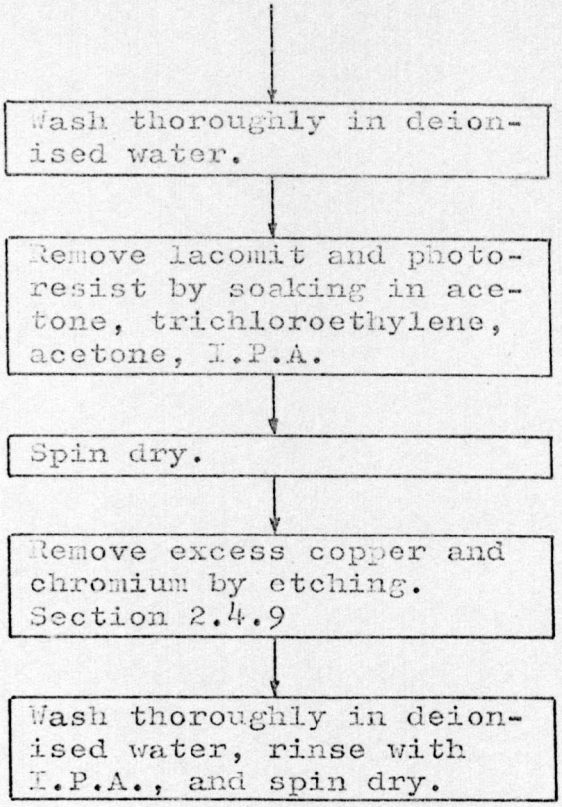
artwork

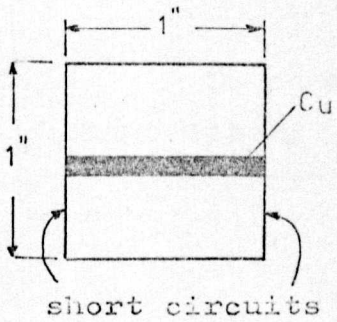


Reduce at 17.5 : 1 using the Wray lens Section 2.3.

mask







FINAL CIRCUIT

The substrates are now ready for use in Mehmet's resonator technique. For use in the nodal shift technique, the samples are modified by removing one of the short circuits. This was most successfully done by polishing the edge with a very fine file. Any attempt at etching would result in severe undercutting of the line.

For T.D.R. measurements, the remaining short circuit is removed in the same way.

APPENDIX 3.2

Derivation of the equation for the locus of the peaks of the nodal shift plot.

From equation 3.8

$$Z_o \tan\beta_o l_o = Z_e \tan\beta_e l_e$$

taking the most significant solution.

For the locus, we require to determine $\frac{dl_o}{df}$. Therefore, differentiating equation 3.8 with respect to f, and assuming that Z_o and Z_e are independent of frequency, to a first order

$$Z_o \sec^2\beta_o l_o \left(\frac{\beta_o l_o}{f} + \beta_o \frac{dl_o}{df}\right) = Z_e \sec^2\beta_e l_e \left(\frac{\beta_e l_e}{f}\right)$$

Therefore

$$\beta_o \frac{dl_o}{df} = \frac{Z_e}{Z_o} \frac{\sec^2\beta_e l_e}{\sec^2\beta_o l_o} \frac{\beta_e l_e}{f} - \frac{\beta_o l_o}{f}$$

$$\frac{dl_o}{df} = \frac{Z_e}{Z_o} \frac{\sec^2\beta_e l_e}{\sec^2\beta_o l_o} \frac{\beta_e l_e}{\beta_o f} - \frac{l_o}{f}$$

The locus of the maxima is given when $\frac{dl_o}{df} = 0$

i.e.
$$\frac{Z_e}{Z_o} \frac{\sec^2\beta_e l_e}{\sec^2\beta_o l_o} \frac{\beta_e l_e}{\beta_o l_o} = 1$$

APPENDIX 3.3

Error analysis of Mehmet's technique for E_{eff}-measurement.

From equation 3.7

$$E_{eff} = \left(\frac{nc}{2fl}\right)^2$$

If σ is the standard deviation, then

$$\sigma^2_{E_{eff}} = \left(\frac{\partial E}{\partial f}eff\right)^2 \sigma_{\bar{f}}^2 + \left(\frac{\partial E}{\partial l}eff\right)^2 \sigma_{\bar{l}}^2$$

$$+ 2\rho_{fl} \frac{\partial E}{\partial l}eff \; \frac{\partial E}{\partial f}eff \; \sigma_{\bar{f}} \sigma_{\bar{l}}$$

where ρ is the correlation coefficient between f and l.

In this case $\rho = 0$, therefore,

$$\sigma^2_{E_{eff}} = \frac{\partial E}{\partial f}^2 eff \; \sigma_{\bar{f}}^2 + \frac{\partial E}{\partial l}^2 eff \; \sigma_{\bar{l}}^2$$

But $$\frac{\partial E}{\partial f}eff = -\frac{2}{f} E_{eff}$$

and $$\frac{\partial E}{\partial l}eff = -\frac{2}{l} E_{eff}$$

Therefore

$$\sigma^2_{E_{eff}} = \frac{4}{f^2} E_{eff}^2 \sigma_{\bar{f}}^2 + \frac{4}{l^2} E_{eff}^2 \sigma_{\bar{l}}^2$$

$$\sigma_{E_{eff}} = 2 \left(\frac{\sigma_{\bar{f}}}{f^2} + \frac{\sigma_{\bar{l}}}{l^2} \right)^{\frac{1}{2}} E_{eff}$$

Error analysis of Mehmet's technique for E_{eff} evaluation

Sample	$\bar{f}_o$	$\frac{\sigma_{\bar{f}}}{\bar{f}}$	$\bar{l}$	$\frac{\sigma_{\bar{l}}}{\bar{l}}$	E_{eff}	$\sigma_{E_{eff}}$	$E_{eff} \pm \sigma_{E_{eff}}$	$E_{eff} \pm \sigma_{E_{eff}}$ %
A	6·433157	9×10^{-5}	25·165	0·00125	3·434	$8·36 \times 10^{-3}$	3·434 ± 0·009	3·434 ± 0·25%
	9·606473	7×10^{-5}			3·467	$8·65 \times 10^{-3}$	3·465 ± 0·009	3·465 ± 0·25%
B	6·609276	$2·8 \times 10^{-6}$	24·783	0·000126	3·301	$0·831 \times 10^{-3}$	3·301 ± 0·0008	3·301 ± 0·025%
	9·870651	$3·0 \times 10^{-6}$			3·33	$0·839 \times 10^{-3}$	3·33 ± 0·0008	3·33 ± 0025
C	6·919439	$2·1 \times 10^{-4}$	24·522	0·00047	3·126	$3·22 \times 10^{-3}$	3·126 ± 0·003	3·126 ± 0·1 %
	10·347759	$1·5 \times 10^{-4}$			3·145	$3·04 \times 10^{-3}$	3·145 ± 0·003	3·145 ± 0·1 %
D	6·817688	$1·5 \times 10^{-4}$	24·972	0·000208	3·105	$1·59 \times 10^{-3}$	3·105 ± 0·002	3·105 ± 0·067%
	10·197018	$1·7 \times 10^{-4}$			3·123	$1·63 \times 10^{-3}$	3·123 ± 0·002	3·123 ± 0·067%
E	6·873104	5×10^{-4}	24·993	0·000173	3·05	$3·23 \times 10^{-3}$	3·05 ± 0·003	3·05 ± 0·1 %
	10·291116	8×10^{-4}			3·061	$5·01 \times 10^{-3}$	3·061 ± 0·005	3·061 ± 0·14 %
F	6·968348	$1·2 \times 10^{-4}$	24·956	0·0016	2·976	$0·956 \times 10^{-2}$	2·976 ± 0·01	2·976 ± 0·33%
	10·436752	$1·4 \times 10^{-4}$			2·985	$0·96 \times 10^{-2}$	2·985 ± 0·01	2·985 ± 0·33%
G	7·286253	$2·3 \times 10^{-4}$	24·128	0·00225	2·912	$1·335 \times 10^{-2}$	2·912 ± 0·013	2·912 ± 0·3 %
	10·914397	2×10^{-4}			2·92	$1·34 \times 10^{-2}$	2·92 ± 0·013	2·92 ± 0·3 %

APPENDIX 3.4

Error analysis of the nodal shift technique for E_{eff} measurement.

From equation 3.9

$$E_{eff} = \left(\frac{mc}{4fl_e}\right)^2$$

Therefore, this is the same form as the equation used in Mehmet's technique, and the expression for the standard deviation $\sigma_{E_{eff}}$ is (Appendix 3.3)

$$E_{eff} = 2\left(\frac{\sigma_f^2}{f^2} + \frac{\sigma_l^2}{l^2}\right)^{\frac{1}{2}} E_{eff}$$

The corresponding figures for the error analysis are given in the table below.

Sample	f (GHz)	$\frac{\sigma_f}{f}$	l_e (mm)	$\frac{\sigma l_e}{l_e}$	E_{eff}	$\sigma_{E_{eff}}$	$E_{eff} \pm \sigma_{E_{eff}}$	$E_{eff} \pm \sigma_{E_{eff}}$ %
1	4·81	± 0·0083	25·165	0·00125	3·45	0·058	3·45 ± 0·058	3·45 ± 1·68%
	6·40	±0·00625	25·165	0·00125	3·47	0·0442	3·47 ± 0·044	3·47 ± 1·28 %
	8·01	±0·005	25·165	0·00125	3·46	0·0357	3·46 ± 0·036	3·46 ± 1·0 %
	9·57	±0·0042	25·165	0·00125	3·49	0·0306	3·49 ± 0·031	3·49 ± 0·9 %
2	5·02	± 0·008	24·783	0·00126	3·27	0·053	3·27 ± 0·05	3·27 ± 1·6 %
	6·65	± 0·006	24·783	0·00126	3·31	0·041	3·31 ± 0·04	3·31 ± 1·2 %
	8·33	± 0·005	24·783	0·00126	3·3	0·033	3·3 ± 0·033	3·3 ± 1%
	9·85	± 0·004	24·783	0·00126	3·4	0·029	3·4 ± 0·03	3·4 ± 0·9 %

APPENDIX 4.1

Derivation of the resonant conditions for the gap discontinuity measurements.

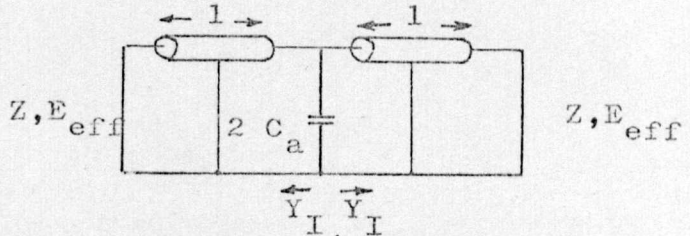


figure A.4.1.1

Input admittance $Y_I = Y \coth \gamma l$

$= Y \coth(\alpha + j\beta)l$

From the mathematical identity[140]

$$\coth(\alpha + j\beta)l = \frac{\sinh 2\alpha l - j \sin 2\beta l}{\cosh 2\alpha l - \cos 2\beta l}$$

For low loss lines $\sinh 2\alpha l \rightarrow 2\alpha l$

$\cosh 2\alpha l \rightarrow 1$

Therefore $$\coth(\alpha + j\beta l) = \frac{2\alpha l - j \sin 2\beta l}{1 - \cos 2\beta l}$$

$$= \frac{2\alpha l - j\, 2 \sin\beta l \cos\beta l}{2 \sin^2 \beta l}$$

$$= \alpha l \operatorname{cosec}^2 \beta l - j \cot \beta l$$

Therefore $Y_I = Y (\alpha l \operatorname{cosec}^2 \beta l - j \cot \beta l)$

At resonance $2\omega C_a - 2 Y \cot \beta l = 0$

Therefore $C_a = \frac{1}{\omega} Y \cot \beta l.$

APPENDIX 4.3

Derivation of the resonant conditions for the gap discontinuity and the gap-and-step discontinuity measurements.

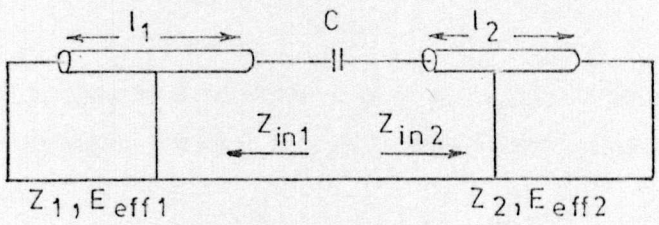


figure A.4.3.1

Input impedance $Z_{in} = Z_o \tanh \gamma l = Z_o \tanh(\alpha + j\beta)l$

But from the mathemetical identity[140]

$$\tanh(\alpha + j\beta)l = \frac{\sinh 2\alpha l + j \sin 2\beta l}{\cosh 2\alpha l + \cos 2\beta l}$$

For low loss lines $\sinh 2\alpha l \longrightarrow 2\alpha l$

$\cosh 2\alpha l \longrightarrow 1$

Therefore $$\tanh(\alpha + j\beta)l = \frac{2\alpha l + j \sin 2\beta l}{1 + \cos 2\beta l}$$

$$= \frac{2\alpha l + j\, 2 \sin\beta l \cos\beta l}{2 \cos^2\beta l}$$

$$\tanh(\alpha + j\beta)l = \alpha l \sec^2\beta l + j \tan\beta l$$

Therefore $$Z_{in} = Z_o(\alpha l \sec^2\beta l + j \tan\beta l)$$

Therefore, in figure A.4.3.1

$$Z_1 \tan\beta_1 l_1 + Z_2 \tan\beta_2 l_2 - \frac{1}{\omega C} = 0$$

i.e. $$C = \frac{1}{\omega} \frac{1}{Z_1 \tan\beta_1 l_1 + Z_2 \tan\beta_2 l_2} \qquad \text{A.4.3.1}$$

For the gap discontinuity, in which $Z_1 = Z_2$, $l_1 = l_2$, $E_{eff1} = E_{eff2}$, and $C = C_b + \frac{C_a}{2}$, then

$$C_b + \frac{C_a}{2} = \frac{1}{\omega} \frac{1}{2 Z \tan\beta l} \qquad \text{A.4.3.2}$$

For the gap-and-step discontinuity, in which $l_1 = l_2$, and $C = C_c$,

$$C_c = \frac{1}{\omega} \frac{1}{Z_1 \tan\beta_1 l + Z_2 \tan\beta_2 l} \qquad \text{A.4.3.3}$$

APPENDIX 4.4

Fabrication of the X band test samples.

The test samples were prepared on 1"x 1"x 0.020" quartz substrates, using copper conductors protected with a gold flash.

Several different fabrication techniques were investigated to obtain the optimum method of manufacturing these circuits, and the technique described below produced the best results, with reference to uniform gap widths, good edge definition, high resonator Q factors and high circuit yields with the minimum of processing stages.

Fabrication process.

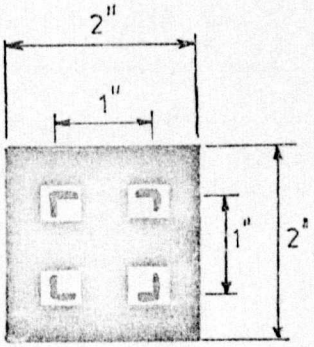
The process described has two major advantages over other practised techniques;

a) the most critical stage (i.e. the formation of the gap), which causes the majority of the rejects, is one of the first stages in the process. In other techniques it is one of the later stages.

b) at the electroplating stage, a uniform current distribution is assured, because of the continuous conducting layer beneath the photoresist layer. Therefore a uniform plating distribution is obtained, which is essential if a uniform gap is to be produced.

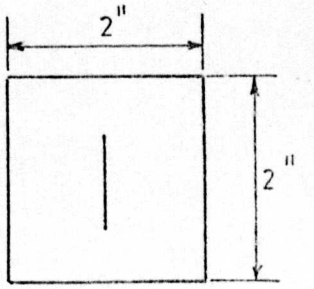
The stages involved in the fabrication are;

1. Clean substrates.
   Section 2.4.2
2. Glow clean substrates.
   Appendix 2.2.
3. Evaporate 200 Å chromium
   1000 Å copper
   over top, bottom and two edges of substrate.
   Section 2.4.3.
4. Apply an 0.6 μm thick layer of Shipley AZ 111 photoresist. Expose and develop alignment mask. Mask substrate back and edges with lacomit.
   Section 2.4.6.



Alignment mask
Reduction 17·5 : 1

5. Etch copper
   Section 2.4.9.
6. Remove photoresist and lacomit by soaking in acetone. Rinse in iso-propyl-alcohol.
7. Apply K.T.F.R.(3 parts)diluted with K.T.F.R. thinner (1 part). Mask back and edges with lacomit. Expose and develop capacitive gap mask.
   Section 2.4.7.



Capacitive gap mask
Reduction 75:1

8. Etch copper and chromium
   Section 2.4.9.

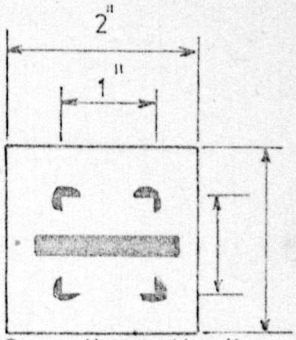
9 Remove the photoresist by soaking in 13LS stripper. Remove lacomit by soaking in acetone. Rinse in I.P.A., and spin dry.

10 Apply a thick layer of K.T.F.R. resist. Expose and develop resonant line mask. Section 2.4.7.

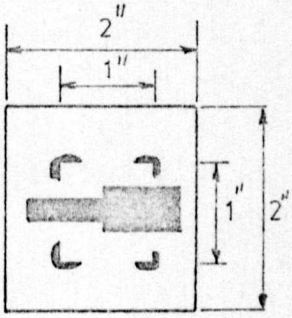
11 Clean back and edges of the substrate with trichloroethylene, acetone and I.P.A.. Soak in Neutra-clean 68. Rinse thoroughly in water. Electroplate to a thickness of 5 μm with copper. Gold flash. Section 2.4.11.

12 Remove photoresist in trichloroethylene. Etch copper and chromium. Section 2.4.9.

13 Rinse in water and I.P.A., and spin dry.



Gap discontinuity mask
Reduction 17·5:1



Gap-and-step discontinuity mask
Reduction 17·5:1

APPENDIX 4.5

Error analysis of the gap discontinuity measurements.

From equation 4.1

$$C_a = \frac{1}{\omega} Y \cot \frac{\omega l \sqrt{E_{eff}}}{c} \qquad A.4.5.1$$

If σ is the standard deviation, then

$$\sigma_{Ca}^2 = \left(\frac{\partial Ca}{\partial f}\right)^2 \sigma_f^2 + \left(\frac{\partial Ca}{\partial Y}\right)^2 \sigma_Y^2 + \left(\frac{\partial Ca}{\partial l}\right)^2 \sigma_l^2 + \left(\frac{\partial Ca}{\partial E_{eff}}\right)^2 \sigma_{E_{eff}}^2$$

where

$$\frac{\partial Ca}{\partial f} = -\frac{Y \cot \frac{\omega l \sqrt{E_{eff}}}{c}}{\omega f} - \frac{Y l \sqrt{E_{eff}}}{fc} \operatorname{cosec}^2 \frac{\omega l \sqrt{E_{eff}}}{c} \qquad A.4.5.2$$

$$\frac{\partial C_a}{\partial Y} = \frac{1}{\omega} \cot \frac{\omega l \sqrt{E_{eff}}}{c} \qquad A.4.5.3$$

$$\frac{\partial C_a}{\partial l} = -\frac{Y \sqrt{E_{eff}}}{c} \operatorname{cosec}^2 \frac{\omega l \sqrt{E_{eff}}}{c} \qquad A.4.5.4$$

$$\frac{\partial C_a}{\partial E_{eff}} = -\frac{Y l}{2c\sqrt{E_{eff}}} \operatorname{cosec}^2 \frac{\omega l \sqrt{E_{eff}}}{c} \qquad A.4.5.5$$

The numerical values of the above partial differentials are calculated from the measured circuit parameters, and the results are summarised in figure A.4.5.1.

Figure A-4-5-1

ERROR ANALYSIS OF THE GAP DISCONTINUITY MEASUREMENTS

Sample	$\frac{\partial C}{\partial f}$	$\frac{\partial C}{\partial Y}$	$\frac{\partial C}{\partial l}$	$\frac{\partial C}{\partial E_{eff}}$	σ_f (Hz)	σ_Y (υ)	σ_l (m)	$\sigma_{E_{eff}}$	σ_{C_a} (pF)	$C_a \pm \sigma_{C_a}$ (pF)	$C_a \pm \sigma_{C_a}$ % (pF)
A	$2 \cdot 37 \times 10^{-22}$	$0 \cdot 32 \times 10^{-12}$	$1 \cdot 87 \times 10^{-10}$	$3 \cdot 64 \times 10^{-13}$	$1 \cdot 0 \times 10^{6}$	$1 \cdot 0 \times 10^{-4}$	$1 \cdot 0 \times 10^{-5}$	$6 \cdot 4 \times 10^{-3}$	0·003	0·01 ± 0·003	0·01 ± 30 %
B	$2 \cdot 39 \times 10^{-22}$	$0 \cdot 29 \times 10^{-12}$	$1 \cdot 88 \times 10^{-10}$	$3 \cdot 66 \times 10^{-13}$	$1 \cdot 0 \times 10^{6}$	$1 \cdot 0 \times 10^{-4}$	$1 \cdot 0 \times 10^{-5}$	$6 \cdot 4 \times 10^{-3}$	0·003	0·0072 ± 0·003	0·0072 ± 42 %
C	$2 \cdot 34 \times 10^{-22}$	$0 \cdot 24 \times 10^{-12}$	$1 \cdot 86 \times 10^{-10}$	$3 \cdot 63 \times 10^{-13}$	$1 \cdot 0 \times 10^{6}$	$1 \cdot 0 \times 10^{-4}$	$1 \cdot 0 \times 10^{-5}$	$6 \cdot 4 \times 10^{-3}$	0·003	0·0076 ± 0·003	0·0076 ± 39 %
D	$2 \cdot 37 \times 10^{-22}$	$0 \cdot 22 \times 10^{-12}$	$1 \cdot 89 \times 10^{-10}$	$3 \cdot 66 \times 10^{-13}$	$1 \cdot 0 \times 10^{6}$	$1 \cdot 0 \times 10^{-4}$	$1 \cdot 0 \times 10^{-5}$	$6 \cdot 4 \times 10^{-3}$	0·003	0·0047 ± 0·003	0·0047 ± 64 %
E	$2 \cdot 42 \times 10^{-22}$	$0 \cdot 19 \times 10^{-12}$	$1 \cdot 91 \times 10^{-10}$	$3 \cdot 7 \times 10^{-13}$	$1 \cdot 0 \times 10^{6}$	$1 \cdot 0 \times 10^{-4}$	$1 \cdot 0 \times 10^{-5}$	$6 \cdot 4 \times 10^{-3}$	0·003	0·0024 ± 0·003	0·0024 ± 125 %
F	$2 \cdot 38 \times 10^{-22}$	$0 \cdot 13 \times 10^{-12}$	$1 \cdot 88 \times 10^{-10}$	$3 \cdot 67 \times 10^{-13}$	$1 \cdot 0 \times 10^{6}$	$1 \cdot 0 \times 10^{-4}$	$1 \cdot 0 \times 10^{-5}$	$6 \cdot 4 \times 10^{-3}$	0·003	0·0045 ± 0·003	0·0045 ± 66 %
G	$2 \cdot 38 \times 10^{-22}$	$0 \cdot 09 \times 10^{-12}$	$1 \cdot 9 \times 10^{-10}$	$3 \cdot 68 \times 10^{-13}$	$1 \cdot 0 \times 10^{6}$	$1 \cdot 0 \times 10^{-4}$	$1 \cdot 0 \times 10^{-5}$	$6 \cdot 4 \times 10^{-3}$	0·003	0·0016 ± 0·003	0·0016 ± 188 %
H	$2 \cdot 37 \times 10^{-22}$	$0 \cdot 054 \times 10^{-12}$	$1 \cdot 88 \times 10^{-10}$	$3 \cdot 66 \times 10^{-13}$	$1 \cdot 0 \times 10^{6}$	$1 \cdot 0 \times 10^{-4}$	$1 \cdot 0 \times 10^{-5}$	$6 \cdot 4 \times 10^{-3}$	0·003	0·0017 ± 0·003	0·0017 ± 176 %

From equation 4.2

$$C_b = \frac{1}{2\omega Z} \cot \beta l - \frac{Ca}{2} \qquad \text{A.4.5.6}$$

Therefore, if σ is the standard deviation, then

$$\sigma_{Cb}^2 = \left(\frac{\partial Cb}{\partial f}\right)^2 \sigma_f^2 + \left(\frac{\partial Cb}{\partial Y}\right)^2 \sigma_Y^2 + \left(\frac{\partial Cb}{\partial l}\right)^2 \sigma_l^2$$

$$+ \left(\frac{\partial Cb}{\partial E_{eff}}\right)^2 \sigma_{E_{eff}}^2 + \left(\frac{\partial Cb}{\partial Ca}\right)^2 \sigma_{Ca}^2$$

where $$\frac{\partial Cb}{\partial f} = -\frac{Y \cot \beta l}{2 \omega f} - \frac{l\sqrt{E_{eff}}\, Y}{2 f c} \operatorname{cosec}^2 \beta l \qquad \text{A.4.5.7}$$

$$\frac{\partial Cb}{\partial Y} = \frac{\cot \beta l}{2 \omega} \qquad \text{A.4.5.8}$$

$$\frac{\partial Cb}{\partial l} = -\frac{\sqrt{E_{eff}}\, Y}{2 c} \operatorname{cosec}^2 \beta l \qquad \text{A.4.5.9}$$

$$\frac{\partial Cb}{\partial E_{eff}} = -\frac{l\, Y}{4 c \sqrt{E_{eff}}} \operatorname{cosec}^2 \beta l \qquad \text{A.4.5.10}$$

$$\frac{\partial Cb}{\partial Ca} = -\tfrac{1}{2} \qquad \text{A.4.5.11}$$

The numerical values of the above partial differentials are calculated from the measured circuit parameters, and the results are summarised in figure A.4.5.2.

Figure A·4·5·2

ERROR ANALYSIS OF THE GAP DISCONTINUITY MEASUREMENTS

Sample	$\frac{\partial C}{\partial f}$	$\frac{\partial C}{\partial Y}$	$\frac{\partial C}{\partial l}$	$\frac{\partial C}{\partial E_{eff}}$	$\frac{\partial C}{\partial C}$	σ_f (Hz)	σ_Y (υ)	σ_l (m)	σ_{Eeff}	σ_{C_a} (pF)	σ_{C_b} (pF)	$C_b \pm \sigma C_b$ (pF)	$C_b \pm \sigma C_b$ % (pF)
A	$1·268 \times 10^{-22}$	$2·02 \times 10^{-12}$	$9·2 \times 10^{-11}$	$1·79 \times 10^{-13}$	0·5	$1·0 \times 10^{6}$	$1·0 \times 10^{-4}$	$1·0 \times 10^{-5}$	$6·4 \times 10^{-3}$	0·003	0·002	0·057 ± 0·002	0·057 ± 3·5 %
B	$1·294 \times 10^{-22}$	$2·09 \times 10^{-12}$	$9·25 \times 10^{-11}$	$1·81 \times 10^{-13}$	0·5	$1·0 \times 10^{6}$	$1·0 \times 10^{-4}$	$1·0 \times 10^{-5}$	$6·4 \times 10^{-3}$	0·003	0·0022	0·06 ± 0·002	0·06 ± 3·7 %
C	$1·299 \times 10^{-22}$	$2·26 \times 10^{-12}$	$9·23 \times 10^{-11}$	$1·8 \times 10^{-13}$	0·5	$1·0 \times 10^{6}$	$1·0 \times 10^{-4}$	$1·0 \times 10^{-5}$	$6·4 \times 10^{-3}$	0·003	0·0021	0·065 ± 0·002	0·065 ± 3·2 %
D	$1·312 \times 10^{-22}$	$2·42 \times 10^{-12}$	$9·31 \times 10^{-11}$	$1·81 \times 10^{-13}$	0·5	$1·0 \times 10^{6}$	$1·0 \times 10^{-4}$	$1·0 \times 10^{-5}$	$6·4 \times 10^{-3}$	0·003	0·0021	0·072 ± 0·002	0·072 ± 2·9 %
E	$1·294 \times 10^{-22}$	$2·4 \times 10^{-12}$	$9·12 \times 10^{-11}$	$1·78 \times 10^{-13}$	0·5	$1·0 \times 10^{6}$	$1·0 \times 10^{-4}$	$1·0 \times 10^{-5}$	$6·4 \times 10^{-3}$	0·003	0·0021	0·07 ± 0·002	0·07 ± 3·0 %
F	$1·371 \times 10^{-22}$	$2·57 \times 10^{-12}$	$9·54 \times 10^{-11}$	$1·87 \times 10^{-13}$	0·5	$1·0 \times 10^{6}$	$1·0 \times 10^{-4}$	$1·0 \times 10^{-5}$	$6·4 \times 10^{-3}$	0·003	0·0022	0·08 ± 0·002	0·08 ± 2·75 %
G	$1·342 \times 10^{-22}$	$2·65 \times 10^{-12}$	$9·4 \times 10^{-11}$	$1·83 \times 10^{-13}$	0·5	$1·0 \times 10^{6}$	$1·0 \times 10^{-4}$	$1·0 \times 10^{-5}$	$6·4 \times 10^{-3}$	0,003	0·0021	0·082 ± 0·002	0·082 ± 2·6 %
H	$1·345 \times 10^{-22}$	$2·94 \times 10^{-12}$	$9·242 \times 10^{-11}$	$1·81 \times 10^{-13}$	0·5	$1·0 \times 10^{6}$	$1·0 \times 10^{-4}$	$1·0 \times 10^{-5}$	$6·4 \times 10^{-3}$	0·003	0·0021	0·09 ± 0·002	0·09 ± 2·33 %

APPENDIX 4.6

Derivation of the equivalent circuit of the gap-and-step discontinuity.

The equivalent circuit[128] of the step discontinuity of figure A.4.6.1 is the series inductor shown in figure A.4.6.2.

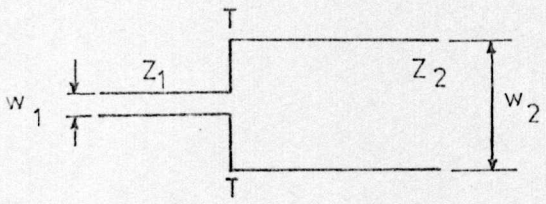


figure A.4.6.1

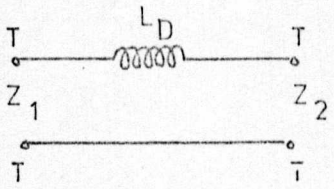


figure A.4.6.2

The equivalent circuit of the gap discontinuity of figure A.4.6.3 has been shown (section 4.3) to be that of figure A.4.6.4

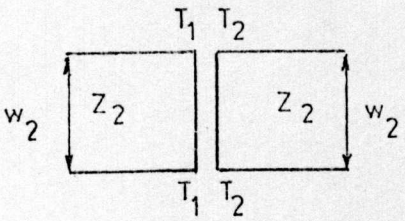


figure A.4.6.3

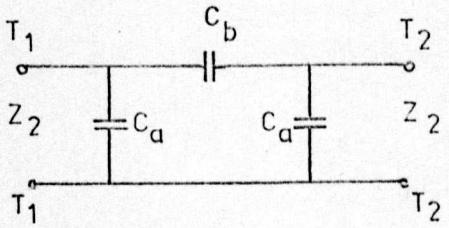


figure A.4.6.4

An equivalent circuit for the combined gap-and-step discontinuity of figure 4.2, is given in figure A.4.6.5.

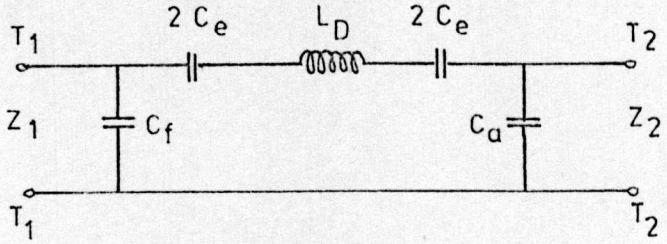


figure A.4.6.5.

This can then be reduced to the circuit of figure A.4.6.6 at any particular frequency.

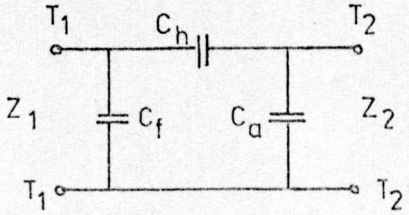


figure A.4.6.6

From the circuits of figure A.4.6.5 and A.4.6.6 it can be deduced that at a constant frequency, ω,

$$C_h = \frac{C_e}{1 - \omega^2 L_D C_E} \qquad \text{A.4.6.1}$$

For the particular gap-and-step discontinuity under consideration

$Z_1 = 50$ ohms

$Z_2 = 32$ ohms

$w_1 = w_2/2$

gap width, s, $\leq$ 50 μm i.e. $s/h \leq 0.1$

From the data quoted by Easter[137] for a step discontinuity in which $w_1 = \frac{w_2}{2}$, at 10 GHz

$$L_D \doteq 0.014 \text{ nH.}$$

From the measured data of the microstrip gap discontinuity of figure 4.16, for $\frac{s}{h} \leq 0.1$, then

$$C_a \leq 0.005 \text{ pF}$$

Since $w_1 = \frac{w_2}{2}$, then to a first approximation, we can assume that

$$C_f \doteq \frac{C_a}{2} \doteq 0.0025 \text{ pF.}$$

The value of C_e of figure A.4.6.5 will be lower than the measured value of C_b shown in figures A.4.6.4 and 4.17, due to the higher effective characteristic impedance of the microstrip line at the gap. Then, to a first approximation, we can assume

$$C_e \doteq 0.05 \text{pF.}$$

Then, very approximately, we can derive from equation A.4.6.1, that at 10 GHz

$$C_h \doteq 0.05 \text{ pF.}$$

The ABCD parameters of the circuit of figure A.4.6.6 are

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 + \frac{C_a}{C_h} & \frac{1}{j\omega C_h} \\ j\omega\left(C_f + C_a + \frac{C_f C_a}{C_h}\right) & 1 + \frac{C_f}{C_h} \end{bmatrix}$$

Substituting the values of C_f, C_h and C_a, as determined above, in the ABCD parameters, we have

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1.1 & -j\ 318 \\ j\ 5 \times 10^{-4} & 1.05 \end{bmatrix}$$

which to a first approximation is equivalent to

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = 1.075 \begin{bmatrix} 1.023 & -j\ 295 \\ 0 & 0.977 \end{bmatrix}$$

which to a first approximation is equivalent to

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = 1.075 \begin{bmatrix} 1 & -j\ 295 \\ 0 & 1 \end{bmatrix}$$

If the impedance of the discontinuity alone is considered, then the ABCD parameters are identical to those of the simple series capacitor of figure A.4.6.7 i.e.

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 & \frac{1}{j\omega C_c} \\ 0 & 1 \end{bmatrix}$$

in which $C_c = 1.075\ C_h$ as shown above.

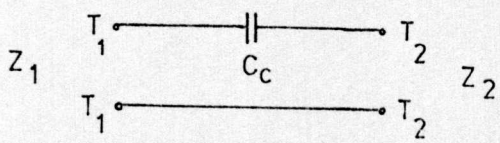


figure A.4.6.7

Therefore, for the particular gap-and-step discontinuity described here, in which $\frac{s}{h} \leq 0.1$, the equivalent circuit of figure A.4.6.5 can, to a first approximation, be simplified to the equivalent circuit of figure A.4.6.7

APPENDIX 4.7

Error analysis of the gap-and-step discontinuity results.

From equation 4.3

$$C_c = \frac{1}{\omega} \frac{1}{Z_1 \tan\beta_1 l + Z_2 \tan\beta_2 l}$$

If σ is the standard deviation, then

$$\sigma_{C_c}^2 = \left(\frac{\partial C_c}{\partial f}\right)^2 \sigma_f^2 + \left(\frac{\partial C_c}{\partial Y_1}\right)^2 \sigma_{Y_1}^2 + \left(\frac{\partial C_c}{\partial Y_2}\right)^2 \sigma_{Y_2}^2$$

$$+ \left(\frac{\partial C_c}{\partial l}\right)^2 \sigma_l^2 + \left(\frac{\partial C_c}{\partial E_{eff1}}\right)^2 \sigma_{E_{eff1}}^2$$

$$+ \left(\frac{\partial C_c}{\partial E_{eff2}}\right)^2 \sigma_{E_{eff2}}^2 \qquad \text{A.4.7.1}$$

where $$\frac{\partial C_c}{\partial f} = -\frac{C_c}{f} - \frac{\omega C_c^2 Z_1 l 2\pi}{v} \sec^2\beta_1 l$$

$$- \frac{\omega C_c^2 Z_2 l 2\pi}{v} \sec^2\beta_2 l \qquad \text{A.4.7.2}$$

$$\frac{\partial C_c}{\partial Y_1} = \omega C_c^2 \frac{\tan\beta_1 l}{Y_1^2} \qquad \text{A.4.7.3}$$

$$\frac{\partial C_c}{\partial Y_2} = \omega C_c^2 \frac{\tan\beta_2 l}{Y_2^2} \qquad \text{A.4.7.4}$$

$$\frac{\partial C_c}{\partial l} = -(\omega C_c)^2 \left(\frac{Z_1}{v_1} \sec^2\beta_1 l + \frac{Z_2}{v_2} \sec^2\beta_2 l\right)$$

A.4.7.5

$$\frac{\partial C_c}{\partial E_{eff1}} = -(\omega C_c)^2 \frac{Z_1 l}{2c\sqrt{E_{eff1}}} \sec^2 \beta_1 l \qquad \text{A.4.7.6}$$

$$\frac{\partial C_c}{\partial E_{eff2}} = -(\omega C_c)^2 \frac{Z_2 l}{2c\sqrt{E_{eff2}}} \sec^2 \beta_2 l \qquad \text{A.4.7.7}$$

The numerical values of the above partial differentials were calculated from the experimental data, and the standard deviation of the capacitance, C_c, was thus determined.

The results are summarised in figure A.4.7.1

FIGURE A-4-7-1

ERROR ANALYSIS OF GAP—AND—STEP DISCONTINUITY MEASUREMENTS

Sample	$\frac{\partial C_c}{\partial f}$	$\frac{\partial C_c}{\partial l}$	$\frac{\partial C_c}{\partial E_{eff1}}$	$\frac{\partial C_c}{\partial E_{eff2}}$	$\frac{\partial C_c}{\partial Y_1}$	$\frac{\partial C_c}{\partial Y_2}$	σ_f (Hz)	σ_l (m)	$\sigma_{E_{eff_1}}$	$\sigma_{E_{eff_2}}$	σ_{Y_1} (υ)	σ_{Y_2} (υ)	σ_C	$C_c \pm \sigma_{C_c}$ (pF)	$C_c \pm \sigma_{C_c}$ % (pF)
1	1.16×10^{-22}	9.06×10^{-11}	5.92×10^{-14}	12.0×10^{-14}	1.26×10^{-12}	0.985×10^{-12}	1.0×10^{6}	1.0×10^{-5}	6.0×10^{-3}	6.4×10^{-3}	0.6×10^{-4}	1.0×10^{-4}	0.00125×10^{-12}	0.054 ± 0.0013	$0.054 \pm 2.4\ \%$
2	1.17×10^{-22}	8.575×10^{-11}	5.72×10^{-14}	11.3×10^{-14}	1.21×10^{-12}	0.904×10^{-12}	1.0×10^{6}	1.0×10^{-5}	6.0×10^{-3}	6.4×10^{-3}	0.6×10^{-4}	1.0×10^{-4}	0.00139×10^{-12}	0.0515 ± 0.0014	$0.0515 \pm 2.7\ \%$
3	1.19×10^{-22}	8.75×10^{-11}	5.775×10^{-14}	11.55×10^{-14}	1.22×10^{-12}	0.93×10^{-12}	1.0×10^{6}	1.0×10^{-5}	6.0×10^{-3}	6.4×10^{-3}	0.6×10^{-4}	1.0×10^{-4}	0.0014×10^{-12}	0.0527 ± 0.0014	$0.0527 \pm 2.6\ \%$
4	1.16×10^{-22}	8.45×10^{-11}	5.575×10^{-14}	11.2×10^{-14}	1.115×10^{-12}	0.852×10^{-12}	1.0×10^{6}	1.0×10^{-5}	6.0×10^{-3}	6.4×10^{-3}	0.6×10^{-4}	1.0×10^{-4}	0.00135×10^{-12}	0.051 ± 0.0014	$0.051 \pm 2.7\ \%$
5	1.015×10^{-22}	7.525×10^{-11}	4.79×10^{-14}	10.1×10^{-14}	0.9475×10^{-12}	0.728×10^{-12}	1.0×10^{6}	1.0×10^{-5}	6.0×10^{-3}	6.4×10^{-3}	0.6×10^{-4}	1.0×10^{-4}	0.0012×10^{-12}	0.044 ± 0.0012	$0.044 \pm 3.2\ \%$
6	1.06×10^{-22}	7.85×10^{-11}	4.89×10^{-14}	10.7×10^{-14}	0.9275×10^{-12}	0.744×10^{-12}	1.0×10^{6}	1.0×10^{-5}	6.0×10^{-3}	6.4×10^{-3}	0.6×10^{-4}	1.0×10^{-4}	0.0012×10^{-12}	0.043 ± 0.0012	$0.043 \pm 2.8\ \%$
7	1.19×10^{-22}	8.975×10^{-11}	4.05×10^{-14}	13.6×10^{-14}	0.685×10^{-12}	0.68×10^{-12}	1.0×10^{6}	1.0×10^{-5}	6.0×10^{-3}	6.4×10^{-3}	0.6×10^{-4}	1.0×10^{-4}	0.0013×10^{-12}	0.035 ± 0.0013	$0.035 \pm 3.7\ \%$

APPENDIX 5.1

Design of a shielding enclosure for 1" x 1" substrates.

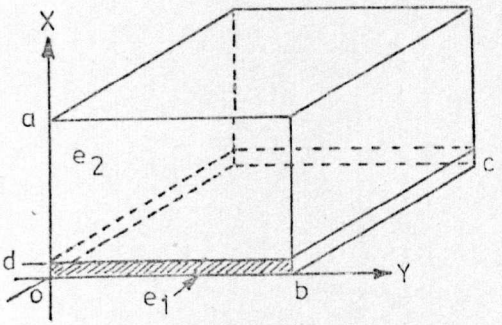


figure A.5.1.1

For a hexahedral cavity in which $c > b > a$, and with d small, the resonant frequency of the dominant mode is given by[157]

$$f_r = f_o \left[1 + \tfrac{1}{2} \left(1 - \frac{e_2}{e_1} \right) \frac{d}{a} \right]$$

where $$f_o = \frac{1}{2\pi \sqrt{e_2 u_o}} \sqrt{\left(\frac{\pi}{b} \right)^2 + \left(\frac{\pi}{c} \right)^2}$$

For the shielding enclosure under consideration

$c = 26\text{mm}$
$b = 25.5\text{mm}$
$a = 5.5\text{mm}$
$d = 0.5\text{mm}$
$e_1 = 3.78$
$e_2 = 1$

and the resonant frequencies can be calculated to be at 8.24 GHz, 16.48 GHz etc.

Therefore, the only box resonance occurring within X band for the shielding enclosure, is at 8.24 GHz.

APPENDIX 5.2.

Microstrip gap equivalent circuit.

The exact equivalent circuit for a gap in microstrip line is shown in figure A.5.2.1

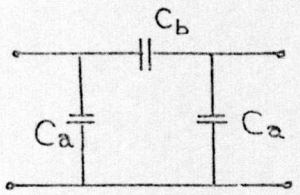


figure A.5.2.1

The ABCD parameters are

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 + \frac{C_a}{C_b} & \frac{1}{j\omega C_b} \\ j\omega C_a\left(2 + \frac{C_a}{C_b}\right) & 1 + \frac{C_a}{C_b} \end{bmatrix}$$

if $C_a = \frac{C_b}{K}$

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 + \frac{1}{K} & \frac{1}{j\omega C_b} \\ \frac{j\omega C_b}{K}\left(2 + \frac{1}{K}\right) & 1 + \frac{1}{K} \end{bmatrix} \qquad \text{A.5.2.1}$$

For a practical microstrip gap in a line of impedance 32 ohms, for $\frac{s}{h} = 0.1$, then from figures 4.23 and 4.24

$$C_a = 0.005 \text{ pF}$$
$$C_b = 0.07 \text{ pF}$$
$$K = 14$$

If $\frac{s}{h} < 0.1$ then $K > 14$

Substituting these values in equation A.5.2.1

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1.07 & -j250 \\ j\ 4\text{x}10^{-4} & 1.07 \end{bmatrix}$$

Therefore, to a first approximation

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 + \frac{1}{K} & \frac{1}{j\,C_b} \\ 0 & 1 + \frac{1}{K} \end{bmatrix}$$

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = (1 + \frac{1}{K}) \begin{bmatrix} 1 & \frac{1}{jC_b(1+1/K)} \\ 0 & 1 \end{bmatrix}$$

which is equivalent, in terms of impedance, to a simple series capacitance, C_g, $(= C_b(1 + 1/K))$, as shown in figure A.5.2.2.

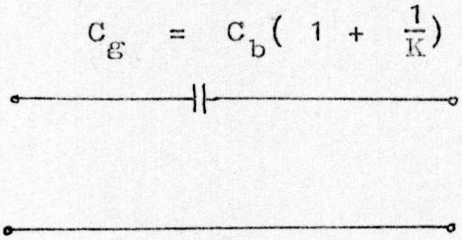


figure A.5.2.2.

APPENDIX 5.3

Equivalent circuit of the test capacitor and microstrip gap.

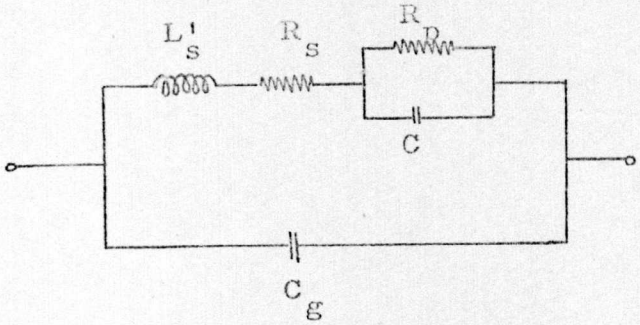


figure A.5.3.1

The equivalent circuit of the test capacitor (omitting for the moment the gap capacitance, C_g) can be reduced to a series R-L-C circuit of impedance Z, given by

$$Z = R_s + j\omega L'_s + \frac{R_p}{1 + j\omega C R_p}$$

If $Q_D = \omega C R_p$ is the dielectric Q factor, then

$$Z = R_s + j\omega L'_s + \frac{R_p(1 - jQ_D)}{1 + Q_D^2}$$

Assuming $Q_D \gg 1$, then

$$Z = R_s + \frac{R_p}{Q_D^2} + j\omega L'_s + \frac{1}{j\omega C}$$

$$Z = R_s + \frac{R_p}{Q_D^2} + \frac{1}{j\omega C}(1 - \omega^2 C L'_s)$$

$$Z = R^* + \frac{1}{j\omega C^*}$$

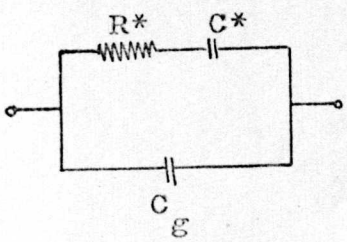


figure A.5.3.2

where $R^* = R_s + \frac{R_p}{Q_D^2}$ A.5.3.1

$$C^* = \frac{C}{1 - \omega^2 C L'_s} \quad \text{A.5.3.2}$$

The capacitor effective Q factor $Q^* = \frac{1}{\omega C^* R^*}$ A.5.3.3

$$Q^* = \frac{1}{\omega C^* (R_s + \frac{R_p}{Q_D^2})}$$

$$\frac{1}{Q^*} = \omega C^* R_s + \frac{\omega C^* R_p}{Q_D^2}$$

$$\frac{1}{Q^*} = \frac{1}{Q_E^*} + \frac{1}{Q_D^*} \quad \text{A.5.3.4}$$

where $Q_E^* = \frac{1}{\omega C^* R_s}$ is the effective electrode Q factor. A.5.3.5

$Q_D^* = \frac{Q_D^2}{\omega C^* R_p}$ is the effective dielectric Q factor A.5.3.6

The capacitor impedance is

$$Z = R^* + \frac{1}{j\omega C^*}$$

therefore

$$Y = \frac{j\omega C^*}{1 + j\omega C^* R^*}$$

$$Y = \frac{j\omega C^* (1 - j\omega C^* R^*)}{1 + (\omega C^* R^*)^2}$$

$$Y = \frac{j\omega C^* (1 - \frac{j}{Q^*})}{1 + (\frac{1}{Q^*})^2}$$

$$Y = j\omega C^* + \frac{\omega C^*}{Q^*}$$

$$Y = \frac{1}{Q^{*2}R^*} + j\omega C^*$$

The admittance of the total circuit, including the gap capacitance, C_g, is

$$Y = \frac{1}{Q^{*2}R^*} + j\omega(C^* + Cg)$$

$$Z = \frac{Q^{*2}R^*}{1 + j\omega(C^* + C_g)Q^{*2}R^*}$$

$$Z = \frac{Q^{*2}R^*(1 - j\omega Q^{*2}R^*(C^* + C_g))}{1 + \omega^2(C^* + C_g)^2 Q^{*4}R^{*2}}$$

$$Z = \frac{Q^{*2}R^*\left(1 - jQ^*\left(\frac{C^* + C_g}{C^*}\right)\right)}{1 + \frac{(C^* + C_g)^2 Q^{*2}}{C^{*2}}}$$

assuming $Q^* \gg 1$

$$Z = \frac{R^*C^{*2}}{(C^* + C_g)^2}\left(1 - j\,Q^*\left(\frac{C^* + C_g}{C^*}\right)\right)$$

$$Z = \frac{R^*C^{*2}}{(C^* + C_g)^2} - j\,\frac{Q^*R^*C^*}{C^* + C_g}$$

$$Z = \frac{1}{Q^*\omega C^*\left(1 + \frac{C_g}{C^*}\right)^2} - j\,\frac{1}{\omega(C^* + C_g)}$$

$$Z = R' + \frac{1}{j\omega C'} \qquad \text{A.5.3.7}$$

which is equivalent to the simple series circuit of figure A.5.3.3

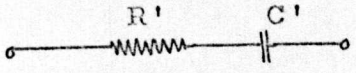


figure A.5.3.3

where $$R' = \frac{1}{Q^* \omega C^* \left(1 + \frac{C_\varepsilon}{C^*}\right)^2} \qquad \text{A.5.3.8}$$

$$C' = C^* + C_\varepsilon \qquad \text{A.5.3.9}$$

APPENDIX 5.4

Derivation of the design equations for the admittance inverter

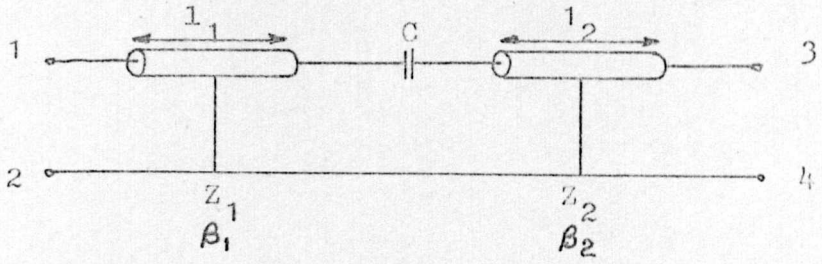


figure A.5.4.1

Assuming the transmission lines are lossless, then, forming the ABCD parameters of the network between terminals 1,2,3 and 4 in figure A.5.4.1

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \cos\beta_1 l_1 & jZ_1 \sin\beta_1 l_1 \\ \frac{j}{Z_1}\sin\beta_1 l_1 & \cos\beta_1 l_1 \end{bmatrix} \begin{bmatrix} 1 & \frac{1}{j\omega C} \\ 0 & 1 \end{bmatrix} \begin{bmatrix} \cos\beta_2 l_2 & jZ_2 \sin\beta_2 l_2 \\ \frac{j}{Z_2}\sin\beta_2 l_2 & \cos\beta_2 l_2 \end{bmatrix}$$

$$= \begin{bmatrix} (\cos\beta_1 l_1 \cos\beta_2 l_2 - \frac{Z_1}{Z_2}\sin\beta_1 l_1 \sin\beta_2 l_2 + \frac{1}{\omega C Z_2}\cos\beta_1 l_1 \sin\beta_2 l_2) & \\ (\frac{j}{Z_1}\sin\beta_1 l_1 \cos\beta_2 l_2 + \frac{j}{\omega C Z_1 Z_2}\sin\beta_1 l_1 \sin\beta_2 l_2 + \frac{j}{Z_2}\cos\beta_1 l_1 \cdot \sin\beta_2 l_2) & \end{bmatrix}$$

$$\begin{bmatrix} (jZ_2 \sin\beta_2 l_2 \cos\beta_1 l_1 + \frac{1}{j\omega C}\cos\beta_1 l_1 \cos\beta_2 l_2 + jZ_1 \sin\beta_1 l_1 \cdot \cos\beta_2 l_2) \\ (-\frac{Z_2}{Z_1}\sin\beta_1 l_1 \sin\beta_2 l_2 + \frac{1}{\omega C Z_1}\sin\beta_1 l_1 \cos\beta_2 l_2 + \cos\beta_1 l_1 \cdot \cos\beta_2 l_2) \end{bmatrix}$$

Consider the admittance inverter of figure A.5.4.2

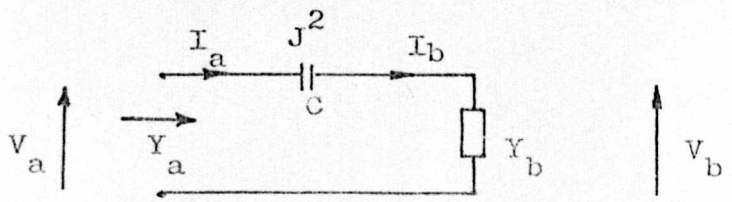


figure A.5.4.2

By definition of the admittance inverter

$$Y_a = \frac{J^2}{Y_b}$$

Forming the ABCD parameters from figure A.5.4.2, then

$$\begin{bmatrix} V_a \\ I_a \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_b \\ I_b \end{bmatrix}$$

$$V_a = AV_b + BI_b$$

$$I_a = CV_b + DI_b$$

$$Y_a = \frac{I_a}{V_a} = \frac{CV_b + DI_b}{AV_b + BI_b} = \frac{C + D\frac{I_b}{V_b}}{A + B\frac{I_b}{V_b}}$$

But $\frac{I_b}{V_b} = Y_b$

Therefore $Y_a = \frac{C + DY_b}{A + BY_b}$

But for a J^2 inverter $Y_a = \frac{J^2}{Y_b}$

therefore $A = D = 0$

$$\frac{C}{B} = J^2$$

Therefore, equating A to zero we have

$$\cos\beta_1 l_1 \cos\beta_2 l_2 - \frac{Z_1}{Z_2}\sin\beta_1 l_1 \sin\beta_2 l_2 + \frac{1}{\omega C Z_2}\cos\beta_1 l_1 \sin\beta_2 l_2 = 0$$

Hence $$\frac{1}{\omega C} = Z_1 \tan\beta_1 l_1 - Z_2 \cot\beta_2 l_2 \qquad \text{A.5.4.1}$$

Similarly, equating D to zero we have

$$\frac{1}{\omega C} = Z_2 \tan\beta_2 l_2 - Z_1 \cot\beta_1 l_1 \qquad \text{A.5.4.2}$$

Also, $J^2 = \frac{C}{B}$

Therefore

$$J^2 = \frac{\frac{\sin\beta_1 l_1 \cos\beta_2 l_2}{Z_1} + \frac{\sin\beta_1 l_1 \sin\beta_2 l_2}{\omega C Z_1 Z_2} + \frac{\cos\beta_1 l_1 \sin\beta_2 l_2}{Z_2}}{Z_2 \sin\beta_2 l_2 \cos\beta_1 l_1 + \frac{1}{\omega C}\cos\beta_1 l_1 \cos\beta_2 l_2 + Z_1 \sin\beta_1 l_1 \cos\beta_2 l_2}$$

$$J^2 = \frac{\sin\beta_1 l_1 \sin\beta_2 l_2 \ (Z_2 \cot\beta_2 l_2 + \frac{1}{\omega C} + Z_1 \cot\beta_1 l_1)}{Z_1 Z_2 \cos\beta_1 l_1 \cos\beta_2 l_2 \ (Z_2 \tan\beta_2 l_2 - \frac{1}{\omega C} + Z_1 \tan\beta_1 l_1)}$$

But from A.5.4.1 $\quad Z_2 \cot\beta_2 l_2 = Z_1 \tan\beta_1 l_1 - \frac{1}{\omega C}$

and from A.5.4.2 $\quad Z_2 \tan\beta_2 l_2 = Z_1 \cot\beta_1 l_1 + \frac{1}{\omega C}$

therefore

$$J^2 = \frac{1}{Z_1 Z_2} \tan\beta_1 l_1 \tan\beta_2 l_2 \ (\frac{Z_1 \tan\beta_1 l_1 + Z_1 \cot\beta_1 l_1}{Z_1 \tan\beta_1 l_1 + Z_1 \cot\beta_1 l_1})$$

therefore

$$J^2 = \frac{\tan\beta_1 l_1 \ \tan\beta_2 l_2}{Z_1 \ Z_2} \qquad \text{A.5.4.3}$$

Now from A.5.4.1 $\quad \frac{1}{\omega C} = Z_1 \tan\beta_1 l_1 - Z_2 \cot\beta_2 l_2$

$$\frac{1}{\omega C} = Z_1 \tan\beta_1 l_1 - \frac{Z_2 \tan\beta_1 l_1}{J^2 Z_1 Z_2}$$

$$\frac{1}{\omega C} = \tan\beta_1 l_1 \ (Z_1 - \frac{1}{J^2 Z_1}) \qquad \text{A.5.4.4}$$

Also from A.5.4.2 $\quad \frac{1}{\omega C} = Z_2 \tan\beta_2 l_2 - Z_1 \cot\beta_1 l_1$

$$\frac{1}{\omega C} = Z_2 \tan\beta_2 l_2 - \frac{Z_1 \tan\beta_2 l_2}{Z_1 Z_2 \cdot J^2}$$

$$\frac{1}{\omega C} = \tan\beta_2 l_2 \ (Z_2 - \frac{1}{J^2 Z_2}) \qquad \text{A.5.4.5}$$

But from A.5.4.3 $\quad \tan\beta_1 l_1 = \frac{J^2 \ Z_1 Z_2}{\tan\beta_2 l_2}$

$$\left(\frac{1}{\omega C}\right)^2 = J^2 Z_1 Z_2 \left(\frac{J^2 Z_1^2 - 1}{J^2 Z_1}\right)\left(\frac{J^2 Z_2^2 - 1}{J^2 Z_2}\right)$$

$$\frac{1}{\omega C} = \frac{1}{J}\left[(J^2 Z_1^2 - 1)(J^2 Z_2^2 - 1)\right]^{\frac{1}{2}} \qquad \text{A.5.4.6}$$

Also from A.5.4.1

$$\frac{1}{\omega C} = Z_1 \tan\beta_1 l_1 - Z_2 \frac{\tan\beta_1 l_1}{J^2 Z_1 Z_2}$$

$$\frac{1}{\omega C} = \frac{J^2 Z_1^2 Z_2 - Z_2}{J^2 Z_1 Z_2} \tan\beta_1 l_1$$

$$\tan\beta_1 l_1 = \frac{J^2 Z_1 Z_2 \left[(J^2 Z_1^2 - 1)(J^2 Z_2^2 - 1)\right]^{\frac{1}{2}}}{Z_2 J (J^2 Z_1^2 - 1)}$$

$$\tan\beta_1 l_1 = Z_1 J \left[\frac{J^2 Z_2^2 - 1}{J^2 Z_1^2 - 1}\right]^{\frac{1}{2}} \qquad \text{A.5.4.7}$$

Similarly it can be shown that

$$\tan\beta_2 l_2 = Z_2 J \left[\frac{J^2 Z_1^2 - 1}{J^2 Z_2^2 - 1}\right]^{\frac{1}{2}} \qquad \text{A.5.4.8}$$

From figure 4.3 it can be seen that the approximate value of C for practical circuits, with $Z_1 = 50$, and $Z_2 = 32$ ohms, is 0.05 pF. Therefore, the approximate value of J^2 at 10 GHz, from equation A.5.4.6, is 1×10^{-5}.

Therefore, from equations A.5.4.7 and A.5.4.8

$\tan\beta_1 l_1$ and $\tan\beta_2 l_2$ are very small (≈ 0.1)

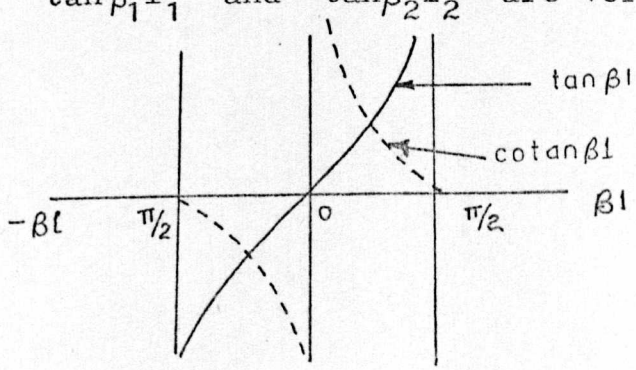


figure A.5.4.3

From figure A.5.4.3 it can be seen that for small values of $\beta 1$

for $\beta 1 > 0$ $\quad \tan\beta 1 > 0$ and small
$\quad \cot\text{an}\beta 1 > 0$ and large

for $\beta 1 < 0$ $\quad \tan\beta 1 < 0$ and small
$\quad \cot\text{an}\beta 1 < 0$ and large

Therefore, from equations A.5.4.1 and A.5.4.2 it can be seen that $\beta 1$ must be negative. i.e. the line lengths, l_1 and l_2, are small and negative.

APPENDIX 5.5

Derivation of the resonance conditions.

Consider the resonant circuit of figure A.5.5.1

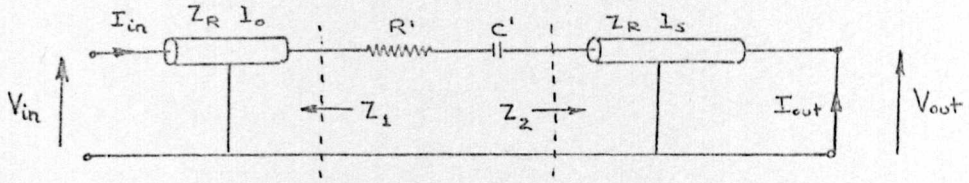


figure A.5.5.1

The impedance looking into the open-circuited length of line is

$$Z_1 = Z_R \coth\gamma l_o = Z_R \left(\frac{\sinh 2\alpha l_o - j \sin 2\beta l_o}{\cosh 2\alpha l_o - \cos 2\beta l_o}\right)$$

For low loss lines, assuming $\alpha l_o \to 0$, then $\sinh\alpha l_o \to \alpha l_o$

$\cosh\alpha l_o \to 1$

then $Z_1 \doteqdot Z_R(\alpha l_o \operatorname{cosec}^2\beta l_o - j\cot\beta l_o)$

Similarly, the impedance Z_2 can be simplified to

$$Z_2 \doteqdot Z_R(\alpha l_s \sec^2\beta l_s + j \tan\beta l_s)$$

The series impedance at the point of connection of the test capacitor is then

$$Z = R' + \frac{1}{j\omega C'} + Z_R(\alpha l_o \operatorname{cosec}^2\beta l_o + \alpha l_s \sec^2\beta l_s + j(\tan\beta l_s - \cot\beta l_o)) \qquad \text{A.5.5.1}$$

At resonance $\mathcal{I}(Z) = 0$

i.e. $$\tan\beta l_s - \cot\beta l_o = \frac{1}{\omega C' Z_R} \qquad \text{A.5.5.2}$$

Forming the ABCD parameters for the overall network

$$\begin{bmatrix} V_{in} \\ I_{in} \end{bmatrix} = \begin{bmatrix} \cosh\gamma l_o & Z_R \sinh\gamma l_o \\ \dfrac{\sinh\gamma l_o}{Z_R} & \cosh\gamma l_o \end{bmatrix} \begin{bmatrix} 1 & R' + \dfrac{1}{j\omega C'} \\ 0 & 1 \end{bmatrix} \begin{bmatrix} \cosh\gamma l_s & Z_R \sinh\gamma l_s \\ \dfrac{\sinh\gamma l_s}{Z_R} & \cosh\gamma l_s \end{bmatrix} \begin{bmatrix} 0 \\ I_{out} \end{bmatrix}$$

Simplifying we obtain

$$\begin{bmatrix} V_{in} \\ I_{in} \end{bmatrix} = \begin{bmatrix} Z_R \cosh\gamma l_o \sinh\gamma l_s + (R' + \frac{1}{j\omega C'})\cosh\gamma l_s \cosh\gamma l_o + \\ \sinh\gamma l_o \sinh\gamma l_s + \frac{1}{Z_R}(R' + \frac{1}{j\omega C'})\cosh\gamma l_s \sinh\gamma l_o + \end{bmatrix}$$

$$\begin{matrix} Z_R \cosh\gamma l_s \sinh\gamma l_o \\ \cosh\gamma l_s \cosh\gamma l_o \end{matrix} \Bigg] \quad I_{out}$$

$$\text{Hence} \qquad Z_{in} = \frac{Z_R(\tanh\gamma l_s + \tanh\gamma l_o) + R' + \frac{1}{j\omega C'}}{1 + \tanh\gamma l_o \tanh\gamma l_s + \frac{1}{Z_R}(R' + \frac{1}{j\omega C'})\tanh\gamma l_o}$$

For low loss lines it has been shown that

$$\tanh\gamma l_s = \alpha l_s \sec^2\beta l_s + j\tan\beta l_s = R_s + jX_s$$

$$\text{and } \tanh\gamma l_o = \alpha l_o \sec^2\beta l_o + j\tan\beta l_o = R_o + jX_o$$

Therefore

$$Z_{in} = \frac{Z_R\ (R_o + R_s + \frac{R'}{Z_R}) + j(X_o + X_s - \frac{1}{\omega C' Z_R})}{1 + R_o R_s - X_o X_s + j(R_o X_s + R_s X_o) + \frac{1}{Z_R}(R_o + jX_o)(R' + \frac{1}{j\omega C'})}$$

$$\frac{Z_{in}}{Z_R} = \frac{1 - \omega C' Z_R(X_o + X_s) + j\omega C'(R' + Z_R(R_o + R_s))}{(R_o - \omega C' R' X_o - \omega C' Z_R(R_s X_o + R_o X_s)) + j(X_o + \omega C' R' R_o + \omega C' Z_R + \omega C' Z_R R_o R_s - \omega C' X_o X_s Z_R)}$$

If $$R_T = 1 - \omega C' Z_R(X_o + X_s) \qquad \text{A.5.5.3}$$

$$X_T = \omega C'(R' + Z_R(R_s + R_o)) \qquad \text{A.5.5.4}$$

$$R_B = R_o - \omega C' R' X_o - \omega C' Z_R(R_s X_o + R_o X_s) \qquad \text{A.5.5.5}$$

$$X_B = X_o + \omega C'R'R_o + \omega C'Z_R + \omega C'Z_R R_o R_s - \omega C'X_o X_s Z_R$$

A.5.5.6

Therefore $$\frac{Z_{in}}{Z_R} = \frac{R_T + j X_T}{R_B + j X_B}$$

$$Y_{in} = \frac{R_B R_T + X_B X_T + j(X_B R_T - X_T R_B)}{Z_R(R_T^2 + X_T^2)}$$

Therefore, at resonance $X_B R_T = X_T R_B$

The real part of the impedance at resonance is

$$R = \frac{Z_R(R_T^2 + X_T^2)}{R_B R_T + X_T^2 \frac{R_B}{R_T}}$$

Hence $$R = Z_R \frac{R_T}{R_B}$$

Expanding, using A.5.5.3 and A.5.5.5

$$R = Z_R \frac{1 - \omega C'Z_R(X_o + X_s)}{R_o - \omega C'R'X_o - \omega C'Z_R(R_s X_o + R_o X_s)}$$

$$R = Z_R \frac{1 - \omega C'Z_R(\tan\beta l_o + \tan\beta l_s)}{\alpha l_o \sec^2\beta l_o - \omega C'R'\tan\beta l_o - \omega C'Z_R(\alpha l_s \sec^2\beta l_s \tan\beta l_o + \alpha l_o \sec^2\beta l_o \tan\beta l_s)}$$

Using equation A.5.5.2 $1 - \frac{\tan\beta l_o + \tan\beta l_s}{\tan\beta l_s - \cot\beta l_o}$

$$R = Z_R \frac{}{\alpha l_o \sec^2\beta l_o - \frac{\tan\beta l_o}{\tan\beta l_s - \cot\beta l_o}\frac{R'}{Z_R} - \frac{\alpha(l_s \sec^2\beta l_s \tan\beta l_o + l_o \sec^2\beta l_o \tan\beta l_s)}{\tan\beta l_s - \cot\beta l_o}}$$

$$R = \frac{Z_R \sec\beta l_o \operatorname{cosec}\beta l_o}{\tan\beta l_o \left(\frac{R'}{Z_R} + \alpha_o (l_s \sec^2\beta l_s + l_o \operatorname{cosec}^2\beta l_o) \right)}$$

let $l_o \operatorname{cosec}^2\beta l_o + l_s \sec^2\beta l_s = m$

Therefore $$R = \frac{Z_R \operatorname{cosec}^2\beta l_o}{\frac{R'}{Z_R} + \alpha_o m} \qquad \text{A.5.5.7}$$

From equation $B = J^2 R Z_I$

Therefore $$B = \frac{J^2 Z_I Z_R \operatorname{cosec}^2\beta l_o}{\frac{R'}{Z_R} + \alpha_o m} \qquad \text{A.5.5.8}$$

From equation A.5.5.1, the Q at resonance, given by[158]

$$Q_o = \frac{\omega_o}{2R} \left. \frac{dX}{d\omega} \right|_{\omega = \omega_o}$$

i.e. $$Q_o = \frac{\omega_o}{2(R' + Z_R \alpha_o m)} \left(Z_R \frac{l_s}{v} \sec^2\beta l_s + \frac{Z_R l_o}{v} \operatorname{cosec}^2\beta l_o + \frac{1}{\omega^2 C'} \right)$$

$$Q_o = \frac{\frac{\omega_o}{2}\left(\frac{l_o}{v} \operatorname{cosec}^2\beta l_o + \frac{l_s}{v} \sec^2\beta l_s + \frac{1}{\omega^2 C' Z_R} \right)}{\frac{R'}{Z_R} + \alpha l_o \operatorname{cosec}^2\beta l_o + \alpha l_s \sec^2\beta l_s}$$

$$Q_o = \frac{\frac{\omega_o}{2}\left(\frac{m}{v} + \frac{1}{\omega^2 C' Z_R} \right)}{\frac{R'}{Z_R} + \alpha m} \qquad \text{A.5.5.9}$$

At the resonant frequency , f_1, with the gap capacitor, C_g, only in the circuit, $R' = 0$

Therefore, from equation A.5.5.8

$$B_1 = \frac{J_1^2 Z_{I1} Z_{R1} \operatorname{cosec}^2\beta_1 l_{o1}}{\alpha_1 m_1} \qquad \text{A.5.5.10}$$

With the test capacitor in the circuit, at the measurement frequency, f_2, from equation A.5.3.8

$$R' = \frac{1}{\omega Q^* C^* \left(1 + \frac{C_g}{C^*}\right)^2}$$

Then from equation A.5.5.8

$$B_2 = \frac{J_2^2 Z_{I2} Z_{R2} \operatorname{cosec}^2 \beta_2 l_{o2}}{\frac{1}{Q^* \omega_2 C^* \left(1 + \frac{C_g}{C^*}\right)^2 Z_{R2}} + \alpha_2 m_2} \qquad \text{A.5.5.11}$$

Rearranging for Q^*

$$Q^* = \frac{B_2}{\omega_2 C^* \left(1 + \frac{C_g}{C^*}\right)^2 Z_{R2}} \cdot \frac{1}{J_2^2 Z_{I2} Z_{R2} \operatorname{cosec}^2 \beta_2 l_{o2} - B_2 \alpha_2 m_2} \qquad \text{A.5.5.12}$$

Substituting for α_2 in equation A.5.5.12 from Appendix 5.6.

$$Q^* = \frac{B_2}{\omega_2 C^* \left(1 + \frac{C_g}{C^*}\right)^2 Z_{R2}} \cdot \frac{1}{J_2^2 Z_{I2} Z_{R2} \operatorname{cosec}^2 \beta_2 l_{o2} - B_2 m_2 \alpha_1 \left(\frac{\omega_2}{\omega_1} \frac{E_{eff2}}{E_{eff1}}\right)^{\frac{1}{2}}}$$

and substituting for α_1 from equation A.5.5.10

$$Q^* = \frac{B_2}{\omega_2 C^* \left(1 + \frac{C_g}{C^*}\right)^2 Z_{R2}} \cdot \frac{1}{J_2^2 Z_{I2} Z_{R2} \operatorname{cosec}^2 \beta_2 l_{o2} - \frac{B_2}{B_1} \frac{m_2}{m_1} \cdot \frac{}{J_1^2 Z_{I2} Z_{R2} \operatorname{cosec}^2 \beta_1 l_{o1} \left(\frac{\omega_2}{\omega_1} \frac{E_{eff2}}{E_{eff1}}\right)^{\frac{1}{2}}}}$$

$$Q^* = \frac{B_2}{J_2^2 Z_{I2} Z_{R2}^2 \operatorname{cosec}^2 \beta_2 l_{o2} \omega_2 C^* \left(1 + \frac{C_f}{C^*}\right)^2} \cdot \frac{1}{1 - \frac{B_2 m_2 Z_{I1} Z_{R1}}{B_1 m_1 Z_{I2} Z_{R2}} \cdot \frac{\sqrt{J_1^2 \operatorname{cosec}^2 \beta_1 l_{o1} \left(\omega_2 E_{effR2}\right)^{\frac{1}{2}}}}{\sqrt{J_2^2 \operatorname{cosec}^2 \beta_2 l_{o2} \left(\omega_1 E_{effR1}\right)^{\frac{1}{2}}}}}$$

$$Q^* = \frac{B_2}{J_2^2 Z_{I2} Z_{R2}^2 \operatorname{cosec}^2 \beta_2 l_{o2} \omega_2 C^* \left(1 + \frac{C_f}{C^*}\right)^2} \cdot$$

$$\cdot \frac{1}{1 - \frac{B_2 m_2 J_1^2 \operatorname{cosec}^2 \beta_1 l_{o1} E_{effR2} \left(\omega_2 E_{effI2}\right)^{\frac{1}{2}}}{B_1 m_1 J_2^2 \operatorname{cosec}^2 \beta_2 l_{o2} E_{effR1} \left(\omega_1 E_{effI1}\right)^{\frac{1}{2}}}}$$

A.5.5.13

APPENDIX 5.6

Variation of resonator conductivity as a function of frequency.

The attenuation of microstrip (α) is due to two sources;

1) the conductor attenuation α_c

2) the substrate dielectric attenuation α_d

and $\alpha = \alpha_c + \alpha_d$

From Appendix 1.3 $\alpha_c \gg \alpha_d$

and therefore $\alpha \doteq \alpha_c$

Now $\alpha_c = \dfrac{R_s}{Z_R w}$

where R_s = the surface resistivity of the conductor, in ohms/square, assuming field penetration to 1 skin depth.

Z_R = resonator characteristic impedance

w = the resonator width

Now $R_s = (\pi f \mu \rho)^{\frac{1}{2}}$

Hence $\alpha = \dfrac{(\pi\mu)^{\frac{1}{2}}}{Z_R w} (f\rho)^{\frac{1}{2}}$

Therefore, if α_1 is the attenuation at frequency f_1

α_2 is the attenuation at frequency f_2

then $\dfrac{\alpha_1}{\alpha_2} = \dfrac{Z_{R2}}{Z_{R1}} \cdot \left(\dfrac{f_1}{f_2}\right)^{\frac{1}{2}} = \left(\dfrac{\omega_1}{\omega_2}\right)^{\frac{1}{2}} \dfrac{Z_{R2}}{Z_{R1}}$

i.e. $\dfrac{\alpha_1}{\alpha_2} = \left(\dfrac{\omega_1}{\omega_2} \dfrac{E_{effR1}}{E_{effR2}}\right)^{\frac{1}{2}}$

APPENDIX 6.1

Determination of the impedance of a capacitor (2D configuration)

The capacitor can be analysed by assuming it is a section of transmission line, of length, l, of which a small section, of length, z, is shown in figure A.6.1.1.

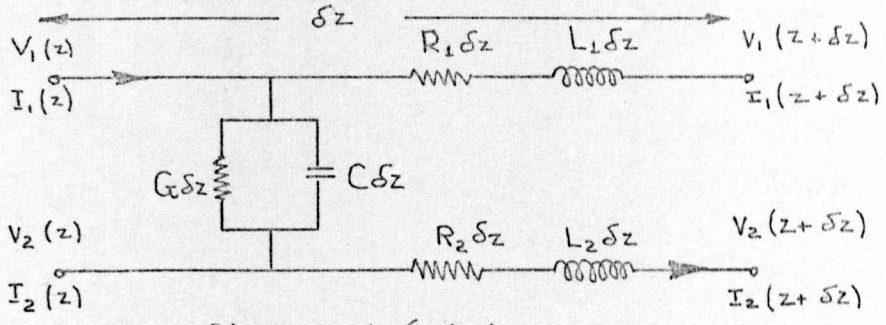


figure A.6.1.1

The transmission line parameters used in figure A.6.1.1 are defined in figure 6.9.

From figure 6.9.a, the boundary conditions are

at $z = 1$ $\quad I_1 = 0$

$\quad\quad I_2 = I_{in} \qquad V_2 = 0$

$z = 0$ $\quad I_1 = I_{in} \qquad V_1 = V_{in}$

$\quad\quad I_2 = 0$

Forming the differential equations, we obtain

$$V_1(z) - V_1(z + \delta z) = I_1(z)\left[R_1\,\delta z + j\omega L_1\,\delta z\right]$$

$$-\frac{dV_1}{dz} = I_1\,(R_1 + j\omega L_1) \qquad \text{A.6.1.1}$$

Similarly $\quad -\dfrac{dV_2}{dz} = I_2\,(R_2 + j\omega L_2) \qquad$ A.6.1.2

$$\left[V_1(z) - V_2(z)\right]\left[G + j\omega C\right] + I_1(z + \delta z) = I_1(z)$$

$$(V_1 - V_2)(G + j\omega C) = -\frac{dI_1}{dz} \qquad \text{A.6.1.3}$$

Similarly

$$(V_1 - V_2)(G + j\omega C) = -\frac{dI_2}{dz} \qquad \text{A.6.1.4}$$

From A.6.1.3 and A.6.1.4

$$\frac{dI_1}{dz} = -\frac{dI_2}{dz} \qquad \text{A.6.1.5}$$

From A.6.1.3

$$\left[\frac{dV_1}{dz} - \frac{dV_2}{dz}\right]\left[G + j\omega C\right] = -\frac{d^2I_1}{dz^2}$$

$$\left[\frac{d^2V_1}{dz^2} - \frac{d^2V_2}{dz^2}\right]\left[G + j\omega C\right] = -\frac{d^3I_1}{dz^3} \qquad \text{A.6.1.6}$$

From A.6.1.1

$$-\frac{d^2V_1}{dz^2} = \frac{dI_1}{dz}(R_1 + j\omega L_1)$$

using A.6.1.5

$$\frac{d^2V_1}{dz^2} = -\frac{dI_1}{dz}(R_1 + j\omega L_1) \qquad \text{A.6.1.7}$$

Similarly, from A.6.1.2

$$\frac{d^2V_2}{dz^2} = \frac{dI_1}{dz}(R_2 + j\omega L_2) \qquad \text{A.6.1.8}$$

Using A.6.1.6, A.6.1.7 and A.6.1.8

$$-\frac{dI_1}{dz}(R_1 + j\omega L_1 + R_2 + j\omega L_2)(G + j\omega C) = -\frac{d^3I_1}{dz^3}$$

Let $r_1 = R_1 + j\omega L_1$ A.6.1.9

$r_2 = R_2 + j\omega L_2$ A.6.1.10

Therefore

$$\frac{d^3I_1}{dz^3} - (r_1 + r_2)(G + j\omega C)\frac{dI_1}{dz} = 0$$

Let $(r_1 + r_2)(G + j\omega C) = \gamma^2$ A.6.1.11

Therefore

$$\frac{d^3I_1}{dz^3} - \gamma^2\frac{dI_1}{dz} = 0$$

Hence $I_1 = A \sinh \gamma z + B \cosh \gamma z + D$ A.6.1.12

From A.6.1.1 and A.6.1.2

$$\frac{dV_1}{dz} - \frac{dV_2}{dz} = I_2(R_2 + j\omega L_2) - I_1(R_1 + j\omega L_1)$$

$$= I_2 r_2 - I_1 r_1$$

From A.6.1.3

$$\frac{dV_1}{dz} - \frac{dV_2}{dz} = - \frac{1}{(G + j\omega C)} \frac{d^2 I_1}{dz^2}$$

$$- \frac{1}{(G + j\omega C)} \frac{d^2 I_1}{dz^2} = I_2 r_2 - I_1 r_1$$

$$I_2 = I_1 \frac{r_1}{r_2} - \frac{1}{(G + j\omega C) r_2} \frac{d^2 I_1}{dz^2}$$

$$= (A \sinh \gamma z + B \cosh \gamma z) \frac{r_1}{r_2} + D \frac{r_1}{r_2}$$

$$- \frac{\gamma^2}{(G + j\omega C) r_2} (A \sinh \gamma z + B \cosh \gamma z)$$

$$I_2 = (A \sinh \gamma z + B \cosh \gamma z)\left(\frac{r_1}{r_2} - \frac{\gamma^2}{(G + j\omega C) r_2} \right)$$

$$+ D \frac{r_1}{r_2}$$

$$I_2 = (A \sinh \gamma z + B \cosh \gamma z)\left(\frac{r_1}{r_2} - \frac{r_1}{r_2} - 1 \right)$$

$$+ D \frac{r_1}{r_2}$$

$$I_2 = - (A \sinh \gamma z + B \cosh \gamma z) + D \frac{r_1}{r_2}$$ A.6.1.13

At $z = 0$ $I_2 = 0$

Therefore $0 = -B + D \frac{r_1}{r_2}$

$$D = B \frac{r_2}{r_1}$$ A.6.1.14

$$I_1 = A \sinh \gamma z + B \cosh \gamma z + B \frac{r_2}{r_1}$$

At $z = 1$ $\quad I_1 = 0$

$$0 = A \sinh \gamma 1 + B \cosh \gamma 1 + B \frac{r_2}{r_1}$$

$$A = \frac{- B}{(\sinh \gamma 1)} \left(\cosh \gamma 1 + \frac{r_2}{r_1}\right) \qquad \text{A.6.1.15}$$

$$I_1 = B\left[\frac{r_2}{r_1} + \cosh \gamma z - \frac{\sinh \gamma z}{\sinh \gamma 1} \left(\cosh \gamma 1 + \frac{r_2}{r_1}\right)\right]$$

A.6.1.16

$$I_2 = B\left[1 - \cosh \gamma z + \frac{\sinh \gamma z}{\sinh \gamma 1} \left(\cosh \gamma 1 + \frac{r_2}{r_1}\right)\right]$$

A.6.1.17

Similarly, setting up the d.e's for V_2 we obtain

$$V_2 = E \sinh \gamma z + F \cosh \gamma z + Gz + H$$

At $z = 1$ $\quad V_2 = 0$

i.e. $\quad H = - (E \sinh \gamma 1 + F \cosh \gamma 1) - G1$

$$V_2 = E(\sinh \gamma z - \sinh \gamma 1) + F(\cosh \gamma z - \cosh \gamma 1) + G(z - 1)$$

Using A.6.1.2

$$- \gamma E \cosh \gamma z - \gamma F \sinh \gamma z - G = B(R_2 + j\omega L_2)\left[1 - \cosh \gamma z + \frac{\sinh \gamma z}{\sinh \gamma 1} \left(\cosh \gamma 1 + \frac{r_2}{r_1}\right)\right]$$

$$= B(R_2 + j\omega L_2) - B \cosh \gamma z (R_2 + j\omega L_2) + \frac{\sinh \gamma z}{\sinh \gamma 1} \left(\cosh \gamma 1 + \frac{r_2}{r_1}\right)(R_2 + j\omega L_2) B$$

Therefore $\quad - \gamma E = B(R_2 + j\omega L_2)$

$$E = B \frac{r_2}{\gamma} \qquad \text{A.6.1.18}$$

Also $$-\gamma F = B\left(\frac{\cosh \gamma l + \frac{r_2}{r_1}}{\sinh \gamma l}\right) r_2$$

$$F = -B\left(\frac{\cosh \gamma l + \frac{r_2}{r_1}}{\sinh \gamma l}\right)\frac{r_2}{\gamma} \qquad \text{A.6.1.19}$$

$$G = -B\,(R_2 + j\omega L_2) \qquad \text{A.6.1.20}$$

Therefore $$V_1 = -\frac{1}{(G + j\omega C)}\frac{dI_1}{dz} + V_2$$

$$= -\frac{1}{(G + j\omega C)} B\gamma\left[\sinh \gamma z - \frac{\cosh \gamma z}{\sinh \gamma l}\left(\frac{r_2}{r_1} + \cosh \gamma l\right)\right] + E(\sinh \gamma z - \sinh \gamma l) +$$

$$F(\cosh \gamma z - \cosh \gamma l) + G(z - 1)$$

$$V_{1\ z=0} = \frac{B\gamma}{(G + j\omega C)}\left(\frac{\cosh \gamma l + \frac{r_2}{r_1}}{\sinh \gamma l}\right) - \sinh \gamma l \frac{B}{\gamma} r_2 -$$

$$\frac{(1 - \cosh \gamma l) B r_2 (\cosh \gamma l + \frac{r_2}{r_1})}{\sinh \gamma l} + Bl\,(R_2 + j\omega L_2)$$

$$= \frac{B}{\gamma \sinh \gamma l}\left[(\cosh \gamma l + \frac{r_2}{r_1})(r_1 + r_2) - r_2\,(1 - \cosh \gamma l)\right.$$

$$\left.(\cosh \gamma l + \frac{r_2}{r_1}) - r_2 \sinh^2 \gamma l + \gamma r_2 \sinh \gamma l\right]$$

$$= \frac{Br_2}{\gamma \sinh \gamma l}\left[\frac{r_1}{r_2}\cosh \gamma l + 2 + \frac{r_2}{r_1}\cosh \gamma l + \gamma l \sinh \gamma l\right]$$

$$= \frac{Br_2}{\gamma \sinh \gamma l}\left[\cosh \gamma l\left(\frac{r_1}{r_2} + \frac{r_2}{r_1}\right) + 2 + \gamma l \sinh \gamma l\right.$$

$$I_{1\ z=0} = B\left(\frac{r_2}{r_1} + 1\right)$$

$$Zin = \frac{r_1 r_2}{(r_1 + r_2)}\frac{1}{\gamma \sinh \gamma l}\left[2 + \cosh \gamma l\left(\frac{r_1}{r_2} + \frac{r_2}{r_1}\right) + \gamma l \sinh \gamma l\right]$$

$$= \frac{r_1 r_2}{r_1 + r_2} l \left[1 + \frac{2}{\gamma l \sinh \gamma l} + \frac{r_1^2 + r_2^2}{r_1 + r_2} \frac{\coth \gamma l}{\gamma} \right]$$

$$Z_{in} = l \left[\frac{r_1 r_2}{r_1 + r_2} \left(1 + \frac{2}{\gamma l \sinh \gamma l} + \frac{r_1^2 + r_2^2}{r_1 + r_2} \frac{\coth \gamma l}{\gamma l} \right) \right]$$

$$Z_{in} = \frac{l}{\gamma} \left[\frac{r_1 \quad r_2}{r_1 + r_2} \left(\gamma l + \frac{2}{\sinh \gamma l} \right) + \frac{r_1^2 + r_2^2}{r_1 + r_2} \coth \gamma l \right]$$

For small γl

$$Z_{in} = \frac{1}{\gamma} \left[\frac{r_1 \quad r_2}{r_1 + r_2} \left(\gamma l + \frac{2}{\gamma l} - \frac{\gamma l}{3} \right) + \frac{r_1^2 + r_2^2}{r_1 + r_2} \left(\frac{1}{\gamma l} + \frac{\gamma l}{3} \right) \right]$$

$$= \frac{1}{\gamma} \left[\frac{\gamma l}{3} (r_1 + r_2) + \frac{1}{\gamma l} (r_1 + r_2) \right]$$

$$Z_{in} = \left[\frac{r_1 + r_2}{3} \right] l + \frac{1}{(G + j\omega C) l}$$

$$Z_{in} = \left[\frac{R_1 + R_2 + j\omega (L_1 + L_2)}{3} \right] l + \frac{1}{(G + j\omega C) l}$$

APPENDIX 7.1

Fabrication of overlay capacitors.

In this Appendix, a process-by-process account is given for the production of overlay capacitors for use in the measurement technique described in Chapter 5. As has been indicated earlier, the fabrication of capacitors for normal circuit applications is a simplification of the process described, and can easily be deduced.

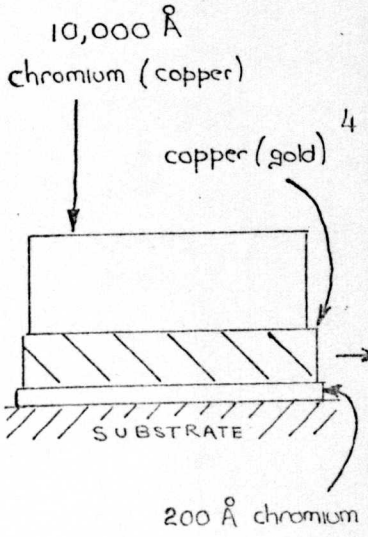
The process described assumes copper electrodes, but the necessary modifications to the process, if gold technology is to be used, are shown in brackets.

Particularly important stages, requiring additional details, refer as necessary, to notes in Appendix 7.2.

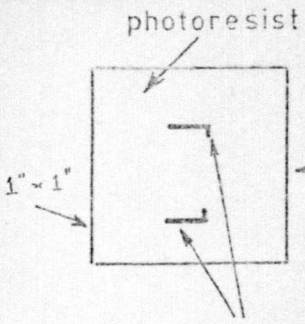
1 Polish substrate edges to remove bevel.

2 Clean substrate.
Section 2.4.2.

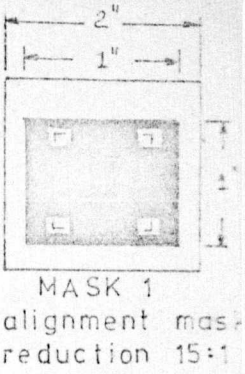
3 Insert substrates in vacuum chamber, using rotational substrate holder. Glow clean.
Appendix 2.2.



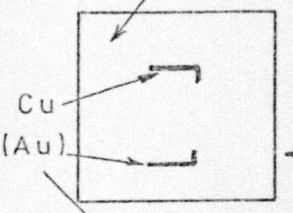
4 Evaporate 200 Å chromium, and copper (gold) to the thickness of the lower electrode, over top and bottom faces, and one edge of the substrate. Evaporate 10,000 Å of chromium (copper) on the top and bottom faces only, as the metal masking layer. (note 1)
Section 2.4.3.



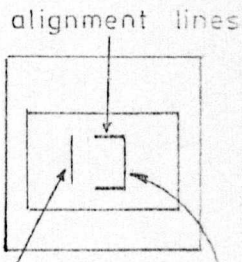
5 Apply 0.6 μm layer of AZ 111 positive photoresist. Expose and develop MASK 1 - alignment mask.
Section 2.4.6.

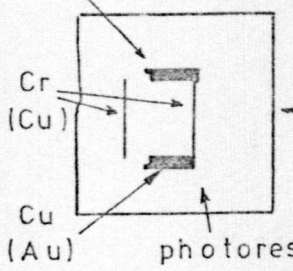


6 Etch chromium (copper)
Section 2.4.9



7 Remove photoresist.
Section 2.4.6.



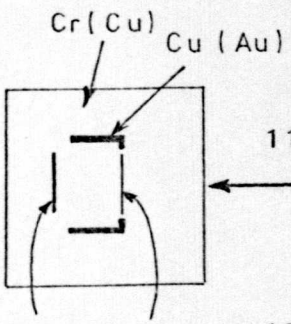


8 Apply 1 μm layer of KTFR. Expose and develop MASK 2, capacitive gap mask.
Section 2.4.7

coupling gap
capacitive gap
MASK 2
gap mask
reduction 60:1

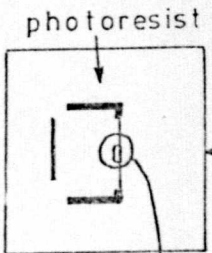
9 Mask rear face and short-circuit edge of substrate with Lacomit.

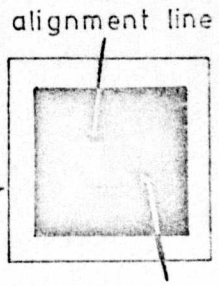
10 Etch chromium (copper), copper (gold) and chromium.
Section 2.4.9.

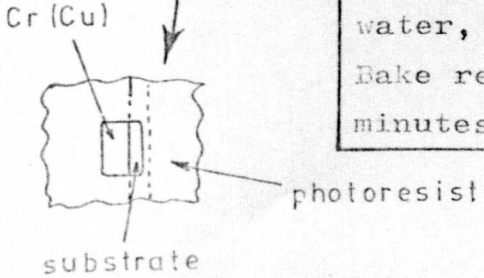


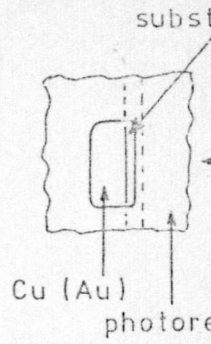
11 Remove Lacomit and resist. Note 2.
Section 2.4.6

12 Apply 15 μm of AZ 111 to top face. Leave at 20°C for 30 minutes. Bake at 70°C for 45 minutes. Align dielectric area mask (MASK 3), and expose for 10 minutes. Develop in AZ 303 developer, diluted 1 part developer to 4 parts water, at 21°C for 5 minutes. Bake resist at 70°C for 60 minutes. Note 3.



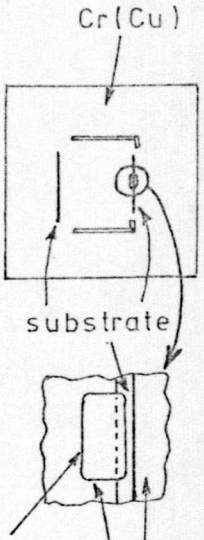






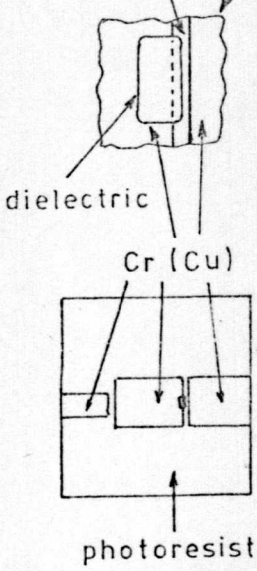
13 Etch chromium (copper). Note 4.
Section 2.4.9.

14 Rinse in filtered water. Blow dry with filtered air. Bake for 15 minutes at 70°C.



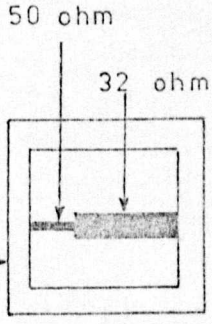
15 Sputter dielectric. Note 5.

16 Soak in acetone until all the resist (and unwanted dielectric) have been removed. Agitate gently as required.



17 Clean in trichloroethylene, Decon 75, water, trichloroethylene, acetone, I.P.A..

18 Apply 2.5 μm of KTFR. Expose and develop resonator mask, MASK 4.
Section 2.4.7.



MASK 4
resonator mask
reduction 15:1

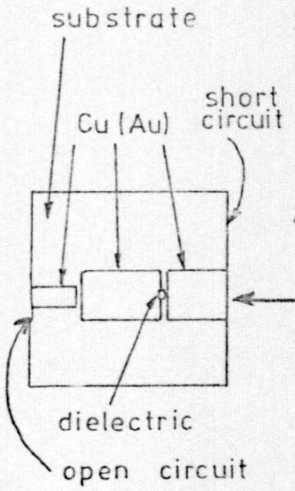
19 Clean bottom face and short circuit edge of substrate with acetone and I.P.A.. Etch chromium (copper). Measure dielectric area and thickness. Clean exposed surfaces thoroughly with Decon 75.

20 Electroplate copper (gold) to 3 μm thickness. Gold flash with 0.1 μm of gold. Note 6.
Section 2.4.11

21 Remove KTFR in trichloro-ethylene, acetone, I.P.A.
Section 2.4.7.

22 Apply Lacomit to capacitor area. Note 7.

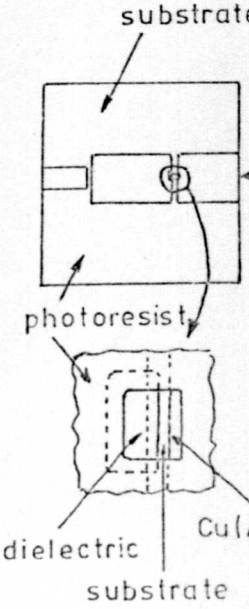
23 Etch chromium (copper), copper (gold), chromium.
Section 2.4.9.



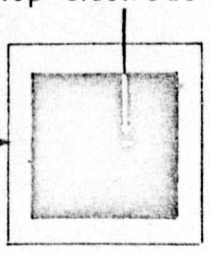
24 Remove Lacomit in acetone and I.P.A.. Clean in Decon 75. Rinse in deionised water and I.P.A.. Spin dry. Measure line dimensions. Measure f_1, Q_1, return loss at resonance.
Chapter 8.

25 Clean thoroughly in trichloro-ethylene, acetone, I.P.A..

26 Evaporate 1000 Å chromium, 1000 Å copper (gold) on the top face of the substrate only. Note 8.



27 Apply 2.5 μm layer of KTFR. Expose and develop top electrode mask (MASK 5). Note 9.
Section 2.4.7.



MASK 5
top electrode mask
reduction 60:1

28 Mask all areas not to be plated using Lacomit.

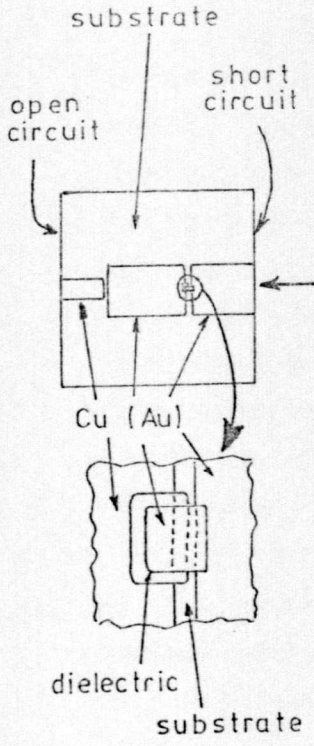
29 Electroplate top electrode, copper with gold flash (gold) to 3 μm thickness. Note 6.
Section 2.4.11.

30 Remove KTFR in trichloroethylene, and Lacomit in acetone. Rinse in trichloroethylene, acetone, and I.P.A..

31 Etch copper (gold) and chromium.
Section 2.4.9

32 Clean in Decon 75, water, I.P.A., spin dry.

33 Measure top electrode dimensions. Measure f_2, Q_2, and return loss at resonance. Chapter 8.



APPENDIX 7.2

Notes on capacitor processing.

1. Metal protective layer

1.1 Material choice.

The main requirement governing the choice of metal protective layer material is that its etchant should not attack the lower electrode material, nor should it unduly weaken the thick photoresist layer. This seemingly simple requirement, in fact, greatly restricts the range of materials open to selection.

If AZ 111 photoresist is used, then strong alkali etchants must be avoided as these soften the photoresist (the developer for AZ 111 is a buffered solution of potassium hydroxide). The use of aluminium as a masking layer was therefore short-lived due to the effect of the etchant (caustic soda). Similarly, if chromium is used as the metal masking layer, it is essential that the sodium hydroxide content of the etchant (Appendix 2.4) is kept strictly to the stated proportions. As the etchant is made freshly before use, however, there should never be any doubt about the exact alkali content.

After considerable experimentation with different materials and etchants, best results were obtained using the following combination of materials.

lower electrode material	masking material	masking material etchant
copper	chromium	ref. Appendix 2.4
gold	copper	ferric chloride ref. Appendix 2.4

1.2 Deposition of the metal protective layer.

The metal layer is deposited at the same time as the initial deposition of the lower electrode material.

This has several significant advantages;

1. the metal protective layer affords immediate protection to the other deposited layers, which is maintained until immediately before the dielectric deposition (for the lower electrode) and immediately before the electroplating stage (for the remainder of the resonant line). This greatly improves the adhesion of the later deposits, and also ensures a higher quality of electroplate because of the uncontaminated surfaces.

2. the microstrip gaps have greatly improved definition due to the metal protective layer acting as an in-contact metal mask. This significantly improved the yield of a previously critical processing stage.

3. the protective layer is extremely useful for defining alignment lines which can be removed at later stages of the process without additional processing stages. In previous techniques, without the metal masking layer, additional processing stages were required to produce the alignment lines.

2. Photoresist removal.

Extreme care should be taken at the resist removal stage, and commercial resist strippers should not be employed. Most commercial strippers are powerful deoxidising agents, and in this application, they remove the oxide layer between the copper and the chromium masking layer, and also remove any additional layers above the protective layer. This feature also applies to commercial cleaning agents which are acid-based, and they should also be avoided at this stage. For resist removal, therefore, the standard solvent techniques should be employed.

3. Photoresist application.

The most crucial stage in the complete process is the formation of the photoresist negative-relief mask.

Initially, KTFR was selected as this would result in the elimination of pinholes in the dielectric due to dust particles on the mask, i.e. in addition to the effects of the metal protective layer. However, the resolution of KTFR decreases with increase in resist thickness, and the desired degree of resolution and dimensional control could not be achieved with the thick resist layers required for the dielectric deposition technique.

AZ 111 resist was therefore adopted, as the resolution is, within certain limits, independent of resist thickness.

Initially, problems were encountered in the production of a uniform 15 μm thick layer of photoresist across a 1" x 1" substrate. Most of the initial techniques attempted produced a build-up of resist at the substrate edges (figure A.7.2.1.a) due to the surface tension at the substrate extremities. This meant that at the photolithographical stages, the mask was not in contact with the photoresist layer at the centre of the substrate, resulting in complete loss of resolution.

Uniform photoresist thickness (figure A.7.2.1.b) was eventually achieved by eliminating the surface tension of the resist at the edges of the substrate. This was accomplished by dip-coating the substrate in the resist, and then placing it, completely immersed in photoresist, on a 2" x 2" glass slide (figure A.7.2.2). After 30 minutes at room temperature, the complete glass slide is transferred to an oven, and the resist is baked at 70°C for 15 minutes. The 1" x 1" substrate is then removed from the glass slide, the rear face is cleaned with acetone, and the substrate is then baked for a further 30 minutes at 70°C. This then results in a uniform thickness of photoresist, as shown in figure A.7.2.1.b.

The extreme thickness of the photoresist layer used, magnifies the variables which affect the dimensional control of the image, and in addition, distorting forces

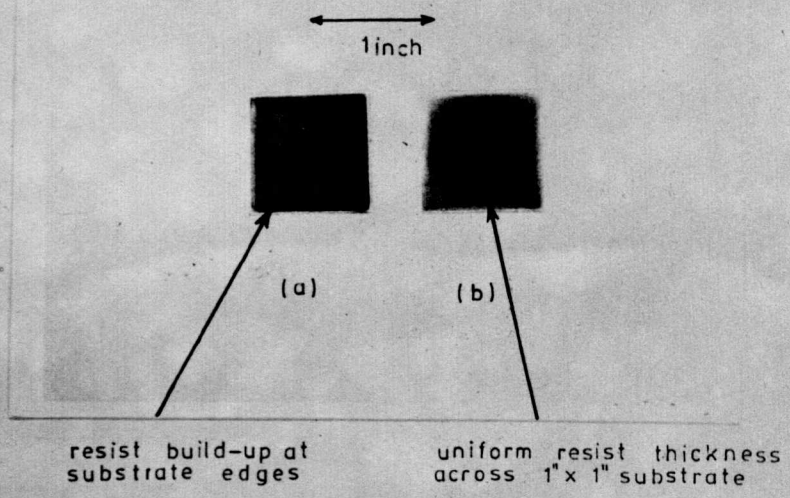


Figure A·7·2·1 Variation in resist thickness

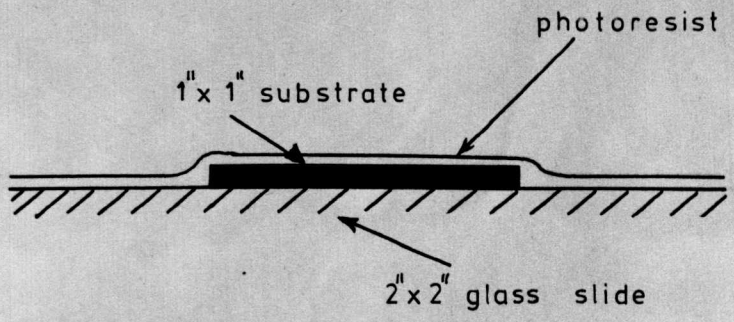


Figure A·7·2·2 Technique for achieving a uniform resist thickness

due to the solvent penetration, are larger, which lead to loss of adhesion, which in itself, is one of the main causes of loss of resolution.

It will be recalled that the dimensional control required for the capacitors used in the resonator technique is relatively demanding. In addition, it was discovered to be extremely important to maintain the profile of the exposed photoresist image as near vertical as possible, otherwise the dielectric would deposit on the sloping photoresist edge and result, either in complete loss of resolution, or in a thick rim of dielectric/photoresist round the outside edge of the dielectric area. To eliminate the latter completely, and to minimise the former, a considerable amount of investigation was carried out to optimise the dimensional control, and it is essential to keep strict control over the photoresist thickness, the exposure times, development times and concentration of developer, and the baking times, if the desired results are to be achieved.

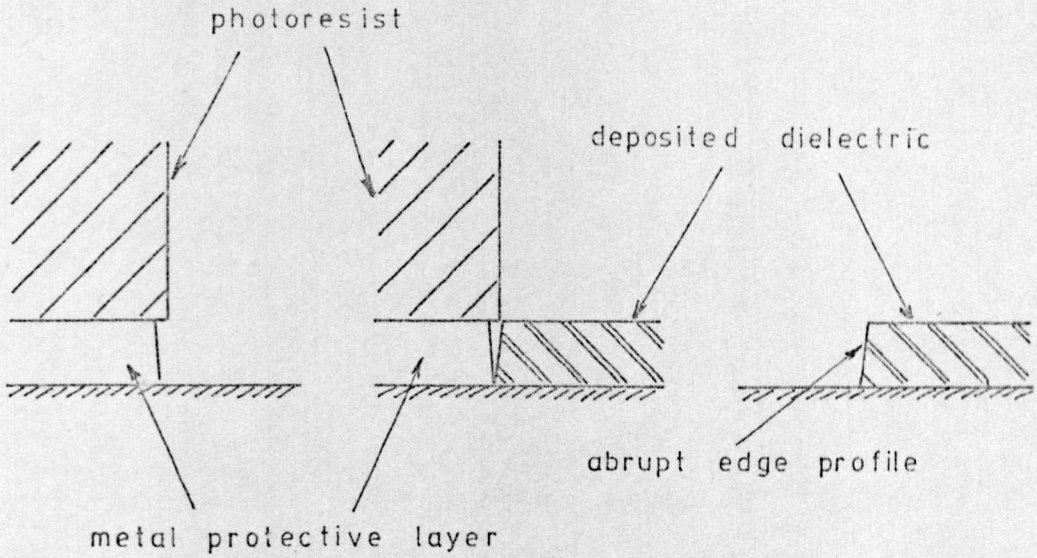
From interferometer studies, it became obvious that even under ideal conditions, the resist profile was far from ideal However, providing the ratio of resist thickness to horizontal displacement of the resist profile is greater than approximately 1 (i.e. an average profile gradient of 45°), then a clean dislocation in the dielectric will result.

However, to achieve the desired results reliably, the procedure laid down above, for the resist deposition, and in Appendix 7.1 for the exposure and development, must be rigidly adhered to.

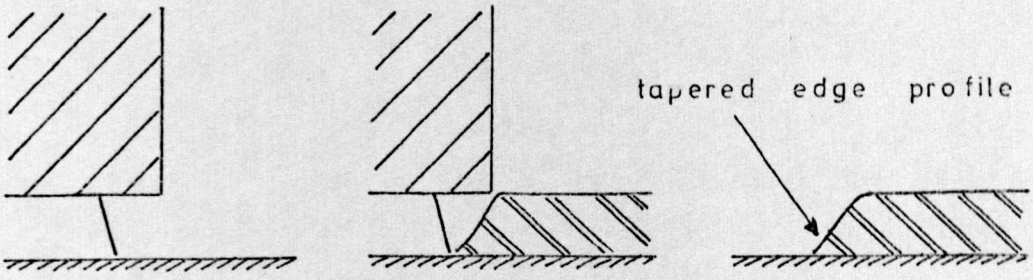
Dielectric edge profile control.

An important advantage of the dielectric deposition technique is that the dielectric edge profile can be carefully controlled to produce an ideal profile for cross-overs and overlays. This is indicated in figure A.7.2.3 which shows that for a metal masking layer thickness approximately equal to the dielectric thickness, a short etching time results in very little undercutting, and an abrupt dielectric edge profile is obtained (figure 7.5).

If the etching time is prolonged, then severe under-



(a) Brief etching time — abrupt edge profile



(b) Prolonged etching — tapered edge profile

Figure A•7•2•3 Dielectric area edge profile control

cutting results, and a tapered profile is obtained (figure 7.4), which is ideal for crossovers.

In practice, the latter is almost always obtained as etching is prolonged in any case, to ensure that all undeveloped particles of resist are removed by undercutting, and that all the metal mask remains are removed.

4. Additional precautions to minimise pinhole formation.

It will be recalled that the prime function of the metal masking layer is the removal of unwanted particles of resist, dust etc, (which would normally produce pinholes in the dielectric), before the dielectric deposition stage.

If, however, contaminants are allowed to deposit on the area where the dielectric is to be deposited, after removal of the protective metal film, then pinholes will still be formed. To prevent this occurrence, it is essential that the following precautions are taken;

a) during removal of the metal masking layer, the etchant should be filtered to 0.1 μm, as should all other substances which may come into contact with the substrate before the dielectric deposition stage and during, or after, the removal of the metal masking layer. The etching must be continued until all particles of the metal masking layer are removed, as all metal particles which remain at this stage will result in the formation of pinholes in the dielectric.

b) the substrate should be carefully protected from atmospheric contamination between the removal of the protective metal layer, and enclosure in the sputtering unit.

c) the sputtering unit should be free from dust, especially the moving parts above the substrate i.e. the shutter. Also, the dielectric target should be pre-sputtered for a minimum of 15 minutes prior to the actual deposition to remove surface contaminants.

5. Dielectric deposition.

During the sputtering stage, the essential requirement is cleanliness of the sputtering system, as dust particles at this stage will result in pinholes in the dielectric.

An additional requirement, which is essential as photoresist is used as the masking material, is that the substrates are kept relatively cool, otherwise carbonisation of the resist will result.

The substrate support (figure A.7.2.4) is water cooled, but to improve heat transfer from the substrate, silicone-grease was applied between the substrate and the substrate support. To minimise the extent to which the photoresist was exposed to the heat from the discharge, a metal mask (figure A.7.2.4) was placed above the substrate, which protected the major area of the photoresist except around a 1mm diameter of the required deposition area. The definition of the dielectric area for the capacitor is still, of course, determined by the photoresist.

The protection of the resist from the radiation of the discharge also permitted rapid removal of the photoresist after the deposition.

6. It will be noted that there is no problem concerning electrical connection to the areas to be plated, due to the continuous conducting layer below the photoresist masking layer.

At the initial plating-up stage (stage 20), pinholes in the dielectric are immediately located. This saves considerable time in the detection of reject capacitors as otherwise the presence of pinholes would not be detected until after the initial microwave measurement, after deposition of the top electrode, and during the second microwave measurement.

For the second plating operation (stage 29) it is essential that a dummy electrode is used, due to the extremely small area of the top electrode.

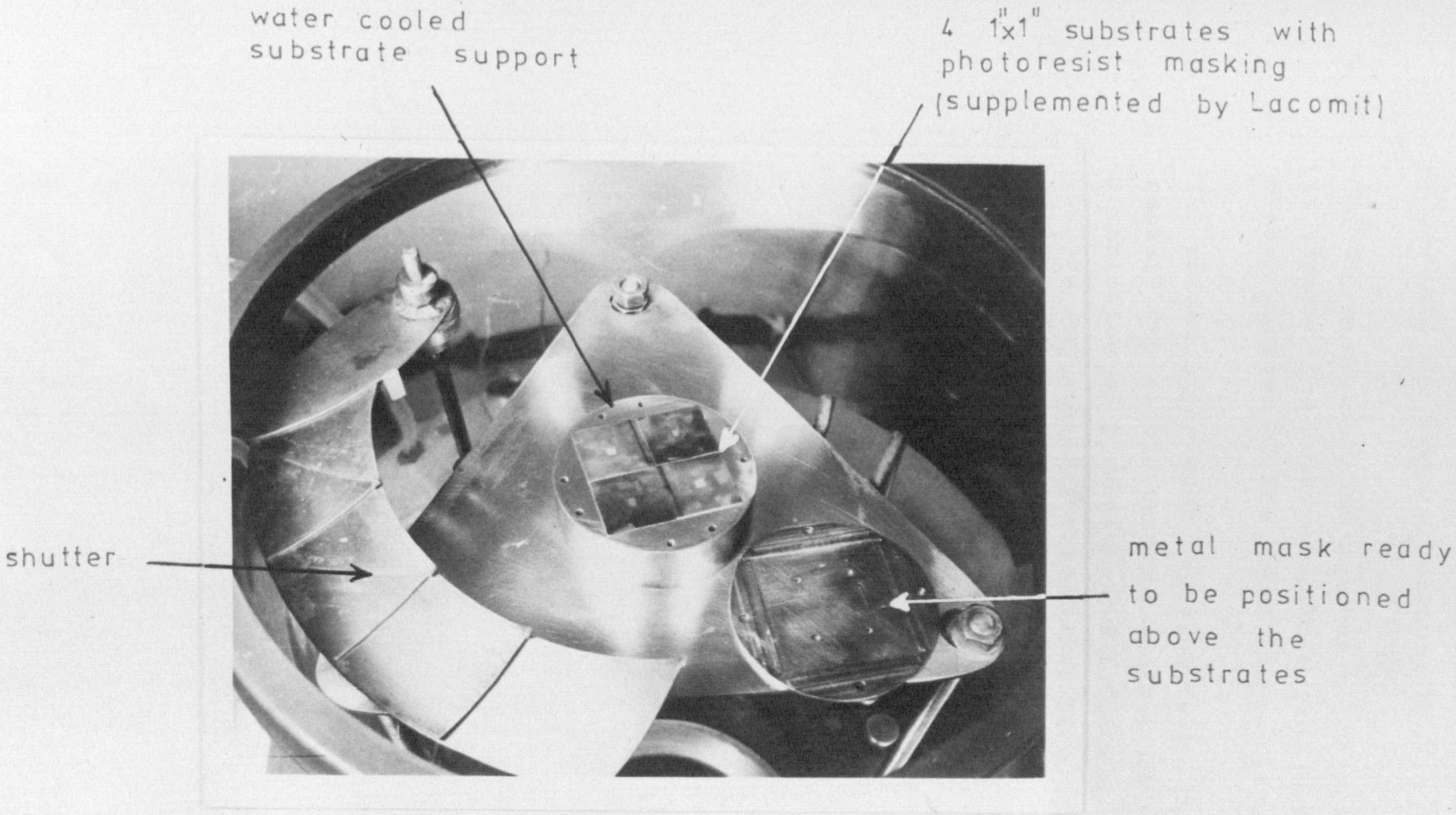


Figure A·7·2·4 Positioning of the substrates in the r.f. sputterer

7. The Lacomit prevents the etchant in stage 23 from attacking the lower electrode.

8. The layer of chromium acts as a protection layer to prevent the lower electrode from being attacked during removal of the copper layer (stage 31).

9. The resist layer must be thick (i.e. full strength resist) due to the surface profile at this stage - a variation of 3 μm from the substrate surface to the top surface of the resonant line.

APPENDIX 8.1

Q factor calculation.

In the Q factor measurement technique, a plot (figure 8.2) of the return loss as a function of frequency, through resonance, is obtained using the reflectometer system of figure 8.1.

The zero dB reference level is obtained by tuning the oscillator off-resonance.

From the resulting calibrated plot, the return loss at resonance is obtained by direct measurement, and the resonant frequency, ω_o, is determined by linear interpolation of the sweep start and stop frequencies.

From the return loss at resonance, the coupling coefficient, B, is obtained from (Appendix 8.2)

$$B\Big|_{\omega = \omega_o} = \frac{1 + e^{\left(-\frac{\text{return loss}}{10}\right)\ln_e 10} \pm 2e^{\left(-\frac{\text{return loss}}{20}\right)\ln_e 10}}{1 - e^{\left(-\frac{\text{return loss}}{10}\right)\ln_e 10}} \qquad \text{A.8.1.1}$$

where + is adopted for the overcoupled circuits ($B > 1$)
and − is adopted for the undercoupled circuits ($B < 1$)

The return loss at the bandwidth points, ω_1 and ω_2, can then be found from (Appendix 8.3)

$$\text{Return loss}\Big|_{\omega = \omega_o \pm \delta\omega} = -10 \log_{10} \frac{(1 - B)^2 + 1}{(1 + B)^2 + 1} \qquad \text{A.8.1.2}$$

The frequencies of the bandwidth points can then be obtained from the calibrated return loss - frequency plot using the calculated values of the return loss at these points. Then, from the measured resonant frequency, ω_o, and the bandwidth, $\delta\omega$, $\left(= \frac{\omega_2 - \omega_1}{2}\right)$, the resonator unloaded Q factor, Q_o, can be obtained from (Appendix 8.3)

$$Q_o = 1 + \frac{\omega_o^2}{\delta\omega\,(2\omega_o + \delta\omega)} \qquad \text{A.8.1.3}$$

APPENDIX 8.2

Derivation of the equation for the coupling coefficient, from the return loss at resonance.

$$\text{Return loss}\Big|_{\omega = \omega_o} = -20 \log_{10} \left|\frac{1 - B}{1 + B}\right|$$

Therefore

$$\left|\frac{1 - B}{1 + B}\right| = e^{-\left(\frac{\text{return loss}}{20}\right) \ln_e 10}$$

$$\frac{1 + B^2 - 2B}{1 + B^2 + 2B} = e^{-\left(\frac{\text{return loss}}{10}\right) \ln_e 10}$$

Rearranging for B we obtain

$$B^2\left(1 - e^{-\frac{\text{return loss}}{10} \ln_e 10}\right) - 2B\left(1 + e^{-\frac{\text{return loss}}{10} \ln_e 10}\right) + 1 - e^{-\frac{\text{return loss}}{10} \ln_e 10} = 0$$

$$B = \frac{2\left(1 + e^{-\frac{\text{return loss}}{10} \ln_e 10}\right) \pm \left[4\left(1 + e^{-\frac{\text{return loss}}{10} \ln_e 10}\right)^2 - 4\left(1 - e^{-\left(\frac{\text{return loss}}{10} \ln_e 10\right)}\right)^2\right]^{1/2}}{2\left(1 - e^{-\frac{\text{return loss}}{10} \ln_e 10}\right)}$$

$$B\Big|_{\omega = \omega_o} = \frac{1 + e^{-\left(\frac{\text{return loss}}{10} \ln_e 10\right)} \pm 2e^{-\left(\frac{\text{return loss}}{20} \ln_e 10\right)}}{1 - e^{-\left(\frac{\text{return loss}}{10} \ln_e 10\right)}} \qquad \text{A.8.2.1}$$

where + is adopted for overcoupled circuits

and − is adopted for undercoupled circuits.

APPENDIX 8.3

Calculation of the Q factor from the return loss at resonance.

Consider the transformed resonant circuit of figure A.8.3.1 (ref. figure 5.20)

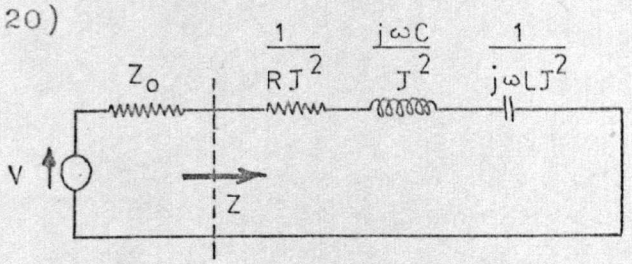


Figure A·8·3·1

The input impedance, Z, of the transformed circuit is

$$Z = \frac{1}{J^2}\left[\frac{1}{R} + j\left(\omega C - \frac{1}{\omega L}\right)\right] \qquad \text{A.8.3.1}$$

At resonance $\omega_o = \frac{1}{\sqrt{LC}}$

and substituting for L in equation A.8.3.1 we obtain

$$Z = \frac{1}{J^2 R}\left[1 + j\,\omega_o CR\left(1 - \frac{\omega_o^2}{\omega^2}\right)\right]$$

From equation

$$B = J^2 R Z_o$$

and also $$Q_o = \omega_o CR$$

Therefore

$$\frac{Z}{Z_o} = \frac{1}{B}\left(1 + j\,Q_o\left(1 - \frac{\omega_o^2}{\omega^2}\right)\right)$$

If ω is defined such that

$$\omega = \omega_o + \delta\omega$$

then

$$1 - \frac{\omega_o^2}{\omega^2} = 1 - \left(\frac{\omega_o}{\omega_o + \delta\omega}\right)^2$$

$$= \frac{\delta\omega\,(2\omega_o + \delta\omega)}{\omega_o(\omega_o + 2\delta\omega) + \delta\omega^2}$$

Therefore

$$\frac{Z}{Z_o} = \frac{1}{B}\left(1 + j\,Q_o \frac{\delta\omega\,(2\omega_o + \delta\omega)}{\omega_o(\omega_o + 2\delta\omega) + \delta\omega^2}\right) \qquad \text{A.8.3.2}$$

The reflection coefficient at any frequency near to resonance is

$$\Gamma = \frac{\frac{Z}{Z_o} - 1}{\frac{Z}{Z_o} + 1} = \frac{1-B + j\,Q_o \dfrac{\delta\omega\,(2\omega_o + \delta\omega)}{\omega_o(\omega_o + 2\delta\omega) + \delta\omega^2}}{1+B + j\,Q_o \dfrac{\delta\omega\,(2\omega_o + \delta\omega)}{\omega_o(\omega_o + 2\delta\omega) + \delta\omega^2}}$$

and the corresponding return loss is

$$\text{Return loss} = -10\log_{10}|\Gamma|^2$$

$$= -10\log_{10} \frac{(1-B)^2 + \left(Q_o \dfrac{\delta\omega(2\omega_o + \delta\omega)}{\omega_o(\omega_o + 2\delta\omega) + \delta\omega^2}\right)^2}{(1+B)^2 + \left(Q_o \dfrac{\delta\omega\,(2\omega_o + \delta\omega)}{\omega_o(\omega_o + 2\delta\omega) + \delta\omega^2}\right)^2} \qquad \text{A.8.3.3}$$

At resonance, $\delta\omega = 0$, and the coupling coefficient is given by equation A.8.2.1.

Therefore, from the measured return loss at resonance, the coupling coefficient, B, is derived using equation A.8.2.1. Then using this value of B in equation A.8.3.3, the return loss at any other frequency, $\omega_o \pm \delta\omega$, can be determined.

If $\delta\omega$ is selected such that

$$Q_o \frac{\delta\omega\,(2\omega_o + \delta\omega)}{\omega_o(\omega_o + 2\delta\omega) + \delta\omega^2} = 1 \qquad \text{A.8.3.4}$$

i.e. $$Q_o = 1 + \frac{\omega_o^2}{\delta\omega(2\omega_o + \delta\omega)} \qquad \text{A.8.3.5}$$

then, from equation A.8.3.3 the return loss is

$$\text{Return loss}\Big|_{\omega = \omega_o \pm \delta\omega} = -10\log_{10} \frac{(1-B)^2 + 1}{(1+B)^2 + 1} \qquad \text{A.8.3.6}$$

APPENDIX 8.4

Microwave measurement technique.

A.8.4.1 Selection of the test equipment.

The measurement system selected must be capable of quickly and accurately measuring the Q factor, return loss and resonant frequency of the test circuit, and the system most suitable for this is a reflectometer.

In general, measurement of the resonant frequency can be performed with ease and accuracy, but the Q factor measurements are considerably more difficult.

The direct measurement of Q was initially attempted in several different ways using the various output devices available (i.e. oscilloscope, polar display, phase-gain indicator, X-Y recorder).

From a series of tests, the two most accurate methods of calculating the Q and resonant frequency were

1) the direct measurement using the polar display and the Q factor overlay [173]

2) using the phase-gain indicator with the X-Y recorder, and calculating the Q factor as described in Appendix 8.1.

The repeatability of each of these methods, for eight observations, was found to be

measurement method	measured Q	measured frequency(GHz)
polar display	374.5 ± 0.32%	11.81739 ± 0.005%
phase-gain indicator	369 ± 0.25%	11.81645 ± 0.0013%

The latter method was finally selected because of

a) the improved reproducibility

b) a direct measurement of the return loss at resonance is also obtained.

The only disadvantages the latter technique has over the former, is the increased measurement time.

A.8.4.2 Reduction of measurement system errors.

The limiting factor in the measurement accuracy of the Q factor, using the technique described in Appendix 8.1, is the variation in the zero dB reference level with frequency. This is of particular importance for the measurements carried out in this thesis, as the resonators are fundamentally low Q, and therefore require a relatively wide frequency sweep for Q measurements ($\approx$100 MHz).

The error in the 0 dB reference level can be significantly reduced if the reflectometer directional couplers are improved in quality, as was evident when the coaxial reflectometer was replaced by the waveguide reflectometer (the variation of return loss with phase was reduced from 1.22dB to 0.39dB for a 1 GHz sweep).

A further reduction in the 0 dB base line variation was achieved by inserting a 5 dB attenuator in the output arm of the isolator (figure 8.1), which increased the isolator return loss from 28 dB to 42 dB.

By a process of elimination, it was established that the directional coupler in the test arm of the reflectometer introduced the most variation in the 0 dB base line with frequency. The directional coupler of the highest quality available was therefore used in this arm (20 dB HP X752D ; directivity - 45 dB at 9000 MHz $\pm$ 100 MHz).

The final variation in the zero dB reference level was 0.09 dB for a 100 MHz sweep about 9000 MHz.

System temperature control.

Tests have shown that the accuracy and repeatability of measurements are very dependent on the stability of the temperature of the equipment (the frequency drift of the oscillator with temperature is 0.01% per degree Centigrade).

The room temperature was therefore maintained constant to within $\pm$ 0.2°C.

To determine the time necessary to allow the equipment to reach an equilibrium temperature, Q measurements were performed (using the technique described in Appendix 8.1) at frequent intervals of time after switching on the equipment. The results were

equipment warm-up time	measured Q factor	Q variation (6 observations)
30 minutes	404	$\pm$ 4.4%
60 minutes	414	$\pm$ 0.49%
120 minutes	401	$\pm$ 0.27%

When the substrate was continually removed from, and replaced in, the shielding enclosure, the repeatability was $\pm$ 0.8% after 120 minutes warm-up. The corresponding repeatability for the resonant frequency measurement was $\pm$ 0.004%.

Shielding enclosure.

It was found to be extremely important to ensure that the shielding enclosure was accurately machined so that

a) the substrate made a good electrical and mechanical contact to the ground plane at the ledges provided (figure 5.27).
b) the substrate did not distort when electrical connection to the microstrip line was made.
c) the shielding enclosure lid was absolutely flat, and did not distort when being secured in position.

A further important factor was the cleanliness of the electrical contact to the microstrip line, and it was found essential to clean the microstrip contact of the APC7 - microstrip connector before every measurement, to ensure that there were no minute particles of metal or quartz adhering to the probe.

A.8.4.3 Measured resonator properties.

It should be noted that the resonator properties are determined to a certain extent by the shielding enclosure. For example, typical results for a resonant line coupled to a 50 ohm line by a capacitor, C_c, resulted in the following measurements, with the lid in position, and with the lid removed.

	resonant frequency (GHz)	Q factor.	return loss	C_c (pF)
with lid	11.677638	359.5	33.9 dB	0.0412
without lid	11.608772	275.5	11.28dB	0.0467

All results quoted refer to the resonators enclosed in a brass cavity, as shown in figure 5.27 with a copper lid. The copper lid was used in preference to brass as the Q factor was increased by typically 8%.

APPENDIX 8.5

Flow diagram for the measurement procedure.

A. Circuit fabrication and microwave measurement.

1 Two opposite edges of a 1"x1"x0.020" quartz substrate are polished (section 3.4.2), and the substrate thickness, h, is measured using a Tesamaster direct reading micrometer.

↓

2 The resonant line, and the capacitor lower electrode and dielectric, are formed, as indicated in Appendix 7.1, stages 1 - 24.

↓

3 The resonant line dimensions (figure A.8.5.1) are measured using a Zeiss toolmaker's microscope.

↓

4 The lower electrode thickness, t_2, (figure A.8.5.2) and the dielectric thickness, t_3, are measured using a Talystep.

↓

5 The resonant frequency, f_1, the Q factor, Q_1, and the return loss at resonance, RLOS1, are measured using the waveguide reflectometer of figure 8.1.

↓

6 The capacitor top electrode is constructed as indicated in Appendix 7.1, stages 25 - 32.

↓

7 The capacitor dimensions (figure A.8.5.3) are measured using an Olympus microscope, with a Filar Micrometer eyepiece attachment.

↓

8 The resonant frequency, f_2, and the return loss at resonance, RLOS2, are then measured for the completed resonator.

↓

9 The top electrode thickness, t_1, (figure A.8.5.4) is measured using a Talystep.

↓

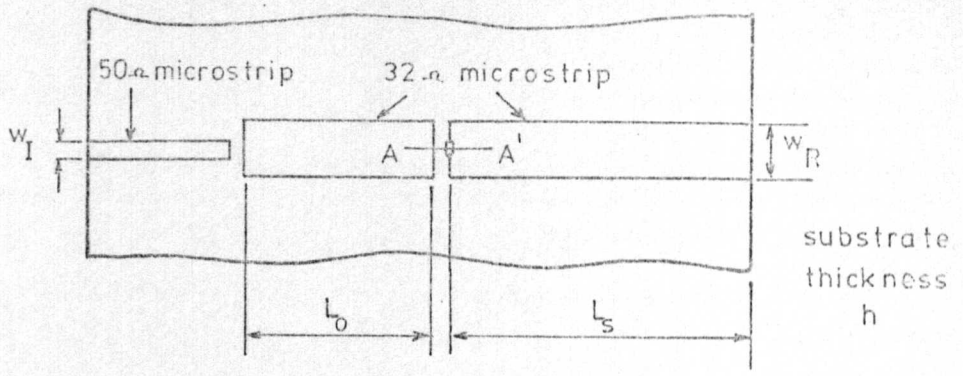


Figure A·8·5·1 Resonator dimensions

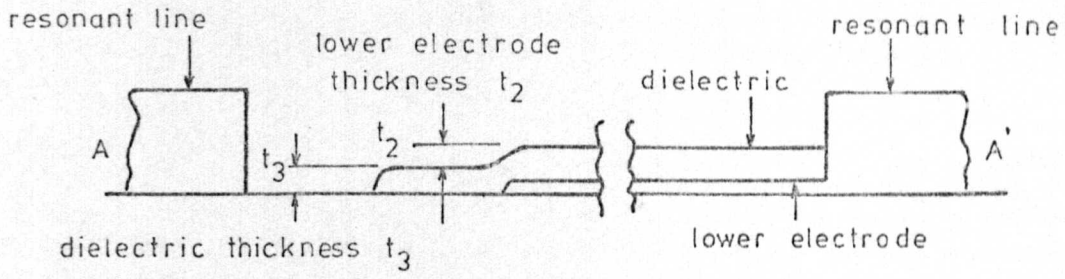


Figure A·8·5·2 Cross-section on AA' of figure A·8·5·1

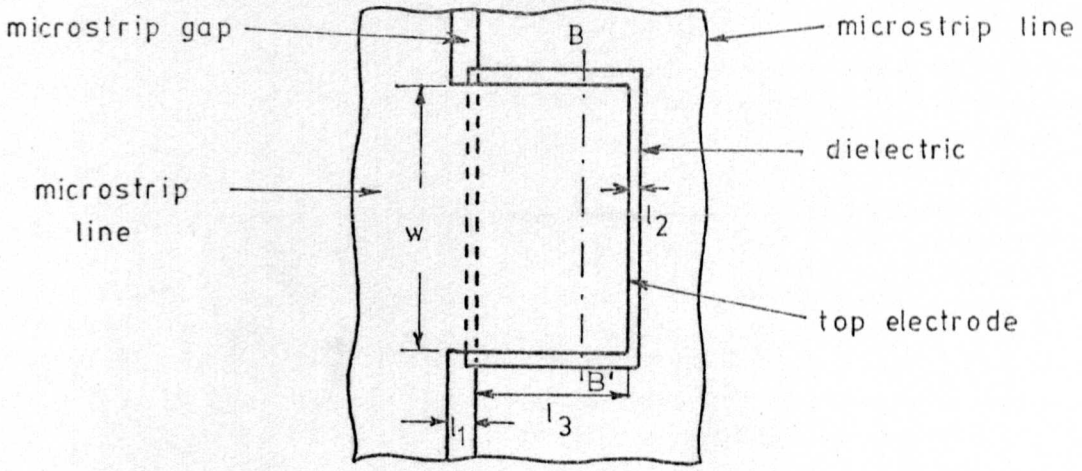


Figure A·8·5·3 Capacitor dimensions

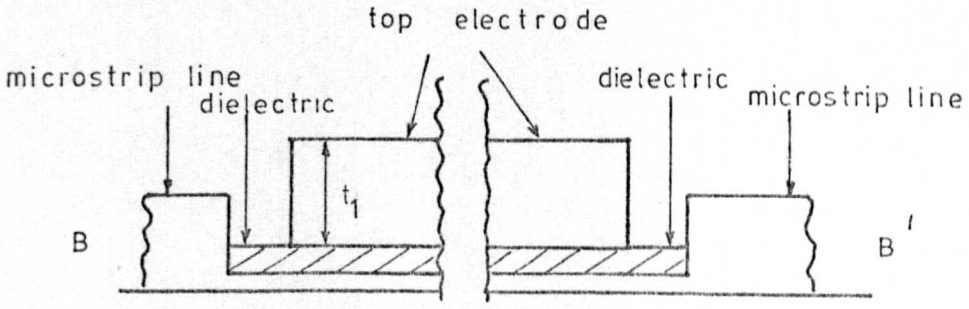


Figure A·8·5·4 Cross section on BB' of figure A·8·5·3

B. Measurement analysis.

10 The effective dielectric constants of the two microstrip lines (i.e. the input line, nominally 50 ohms, and the resonant line, nominally 32 ohms) at the two measurement frequencies, f_1 and f_2, are calculated (Appendix 8.6) from the previously measured data given in figure 3.12.

↓

11 The exact impedances of the two lines at the two measurement frequencies are then calculated (Appendix 8.6.2)

↓

12 From the measured values of return loss (RLOS1), and Q factor (Q1), the coupling capacitance, C_c, and the line attenuation, α_1, are determined (Appendices 8.6.3 - 8.6.5)

↓

13 From the measured resonant frequency, f_1, the gap capacitance, C_g, is determined (Appendices 8.6.6-8.6.8

↓

14 From the known line attenuation, α_1, at frequency, f_1, the line attenuation, α_2, at frequency, f_2, can be calculated (Appendix 5.6)

↓

15 From the measured resonant frequency, f_2, and the calculated gap capacitance, C_g, the effective capacitance of the test capacitor, C*, can be determined (Appendix 8.6.8)

↓

16 From the measured return loss, RLOS2, the effective capacitor Q factor, Q*, can be determined (Appendix 8.6.9

↓

17 From the measured dimensions of the capacitor, the electrode inductance, L'_s, is calculated (Appendix 8.6.8

↓

18 From the effective test capacitance, C*, the electrode inductance, L'_s, and the capacitor dimensions, the actual test capacitance, C, and the dielectric constant, e_d, can be determined (Appendices 8.6.8-8.6.

↓

19 - From the dimensions of the capacitor electrodes, and the conductivities of the electrode materials, (obtained from Butlin[7]), the effective electrode Q factor, Q_E^*, is determined (Appendix 8.6.10)

20 From the effective capacitor Q factor, Q^*, and the effective electrode Q factor, Q_E^*, the effective dielectric Q factor, Q_D^*, is determined, and hence the dielectric Q factor, Q_D is obtained. (Appendix 8.6.10)

APPENDIX 8.6

Flow line diagrams for the measurement analysis program.

A.8.6.1 Data input.

a) Resonator dimensions (figure A.8.5.1)

substrate thickness (h)	: H	
input line width (w_I)	: WI	
resonator line width (w_R)	: WR	
resonator line length (L_c)	: ENGOP	
resonator line length (L_s)	: ENGS	

b) Microwave parameters.

First measurement.

resonant frequency (f_1)	: F1	
Q factor (Q_1)	: Q1	
return loss	: RLOS1	- undercoupled
		+ overcoupled

Second measurement.

resonant frequency (f_2)	: F2	
Q factor (Q_2)	: Q2	
return loss	: RLOS2	- undercoupled
		+ overcoupled

c) Capacitor dimensions (figures A.8.5.2 - A.8.5.4)

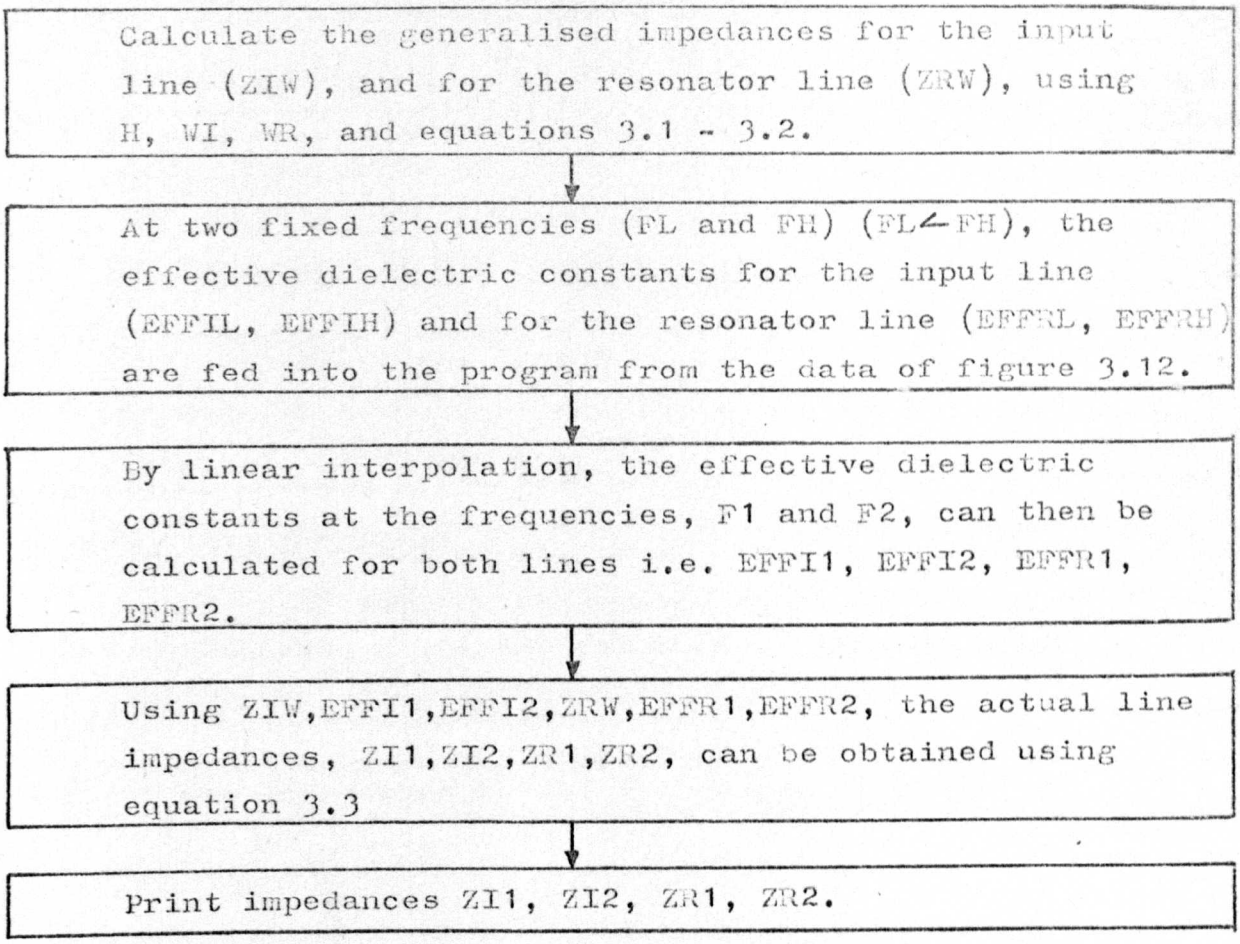
top electrode width (w)	: TWID
top electrode length (l_1)	: WEN1
top electrode thickness (t_1)	: TDEP
capacitor width (w)	: CWID
capacitor length (l_3)	: WEN3
capacitor dielectric thickness (t_3)	: CDEP
lower electrode width (w)	: BWID
lower electrode length (l_2)	: WEN2
lower electrode thickness (t_2)	: BDEP

d) Electrode conductivities.

top electrode conductivity (σ_1)	: CONT
lower electrode conductivity (σ_2)	: CONB

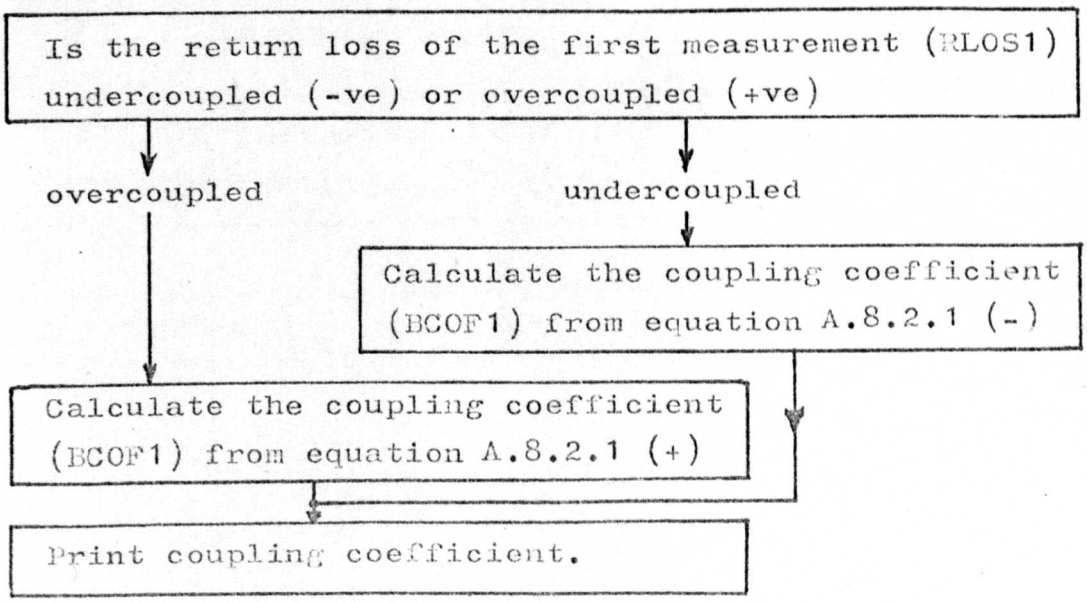
A.8.6.2 Characteristic impedance calculation.

Subroutine IMP



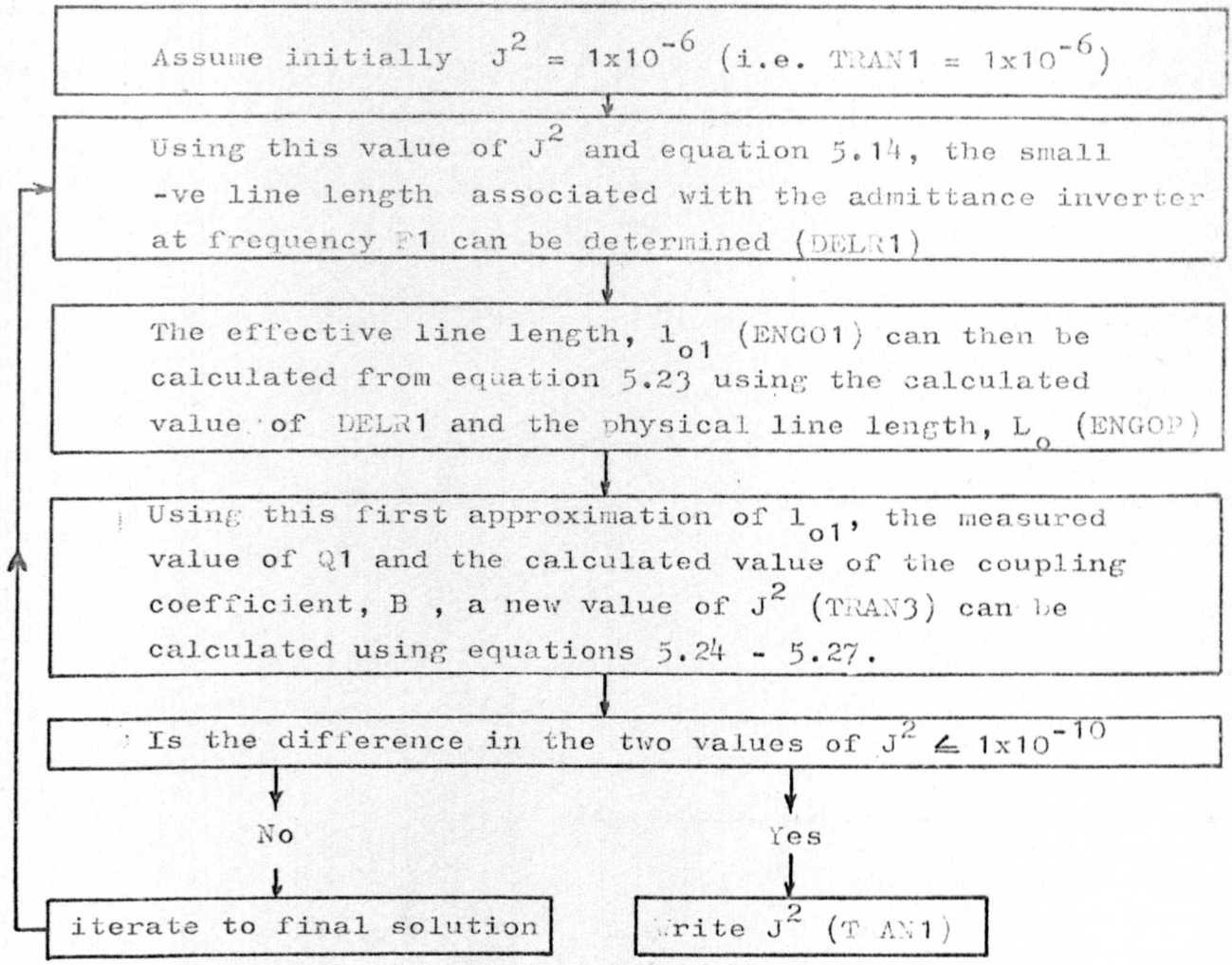
A.8.6.3 Calculation of the coupling coefficient, B , from the return loss.

Subroutine COUPL (RLOS)



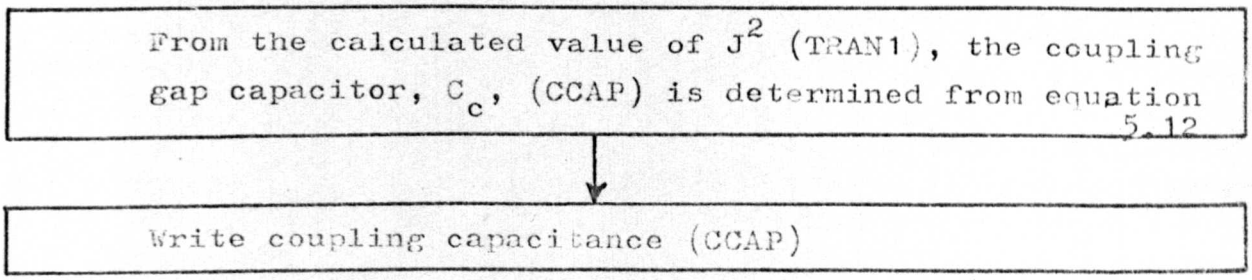
A.8.6.4 Calculation of the admittance inverter parameter J^2 (TRAN1)

Subroutine TRANS



A.8.6.5 Coupling capacitor determination.

Subroutine COUPC.



A.8.6.6 Determination of the effective line lengths, l_{o1}, l_{o2}.
Subroutine DEL(CCAP)

From the calculated value of J^2 (TRAN1), the -ve line length associated with the resonator side of the admittance inverter (DELR1) at frequency F1 is determined from equation 5.14

↓

The effective line length, l_{o1}, (ENGO1) is then calculated from equation 5.23

↓

The value of J^2 at the frequency, f_2, (TRAN2) can then be calculated from equation 5.12 knowing the calculated value of the coupling capacitance, CCAP.

↓

Write J^2 at frequency f_2 (TRAN2).

↓

From the calculated values of J^2 (TRAN2), the -ve line length associated with the resonator side of the admittance inverter (DELR2) at frequency F2 is determined from equation 5.14

↓

The effective line length l_{o2} (ENGO2) is then calculated from equation 5.23

↓

Print the effective line lengths l_{o1} (ENGO1), l_{o2} (ENGO2)

A.8.6.7 Calculation of the coupling coefficient from the return loss
Subroutine COUPL (RLOS)

Is the return loss (RLOS2) undercoupled (-ve) or over-coupled (+ve)

undercoupled → Calculate the coupling coefficient (BCOF2) from equation A.8.2.1 (-)

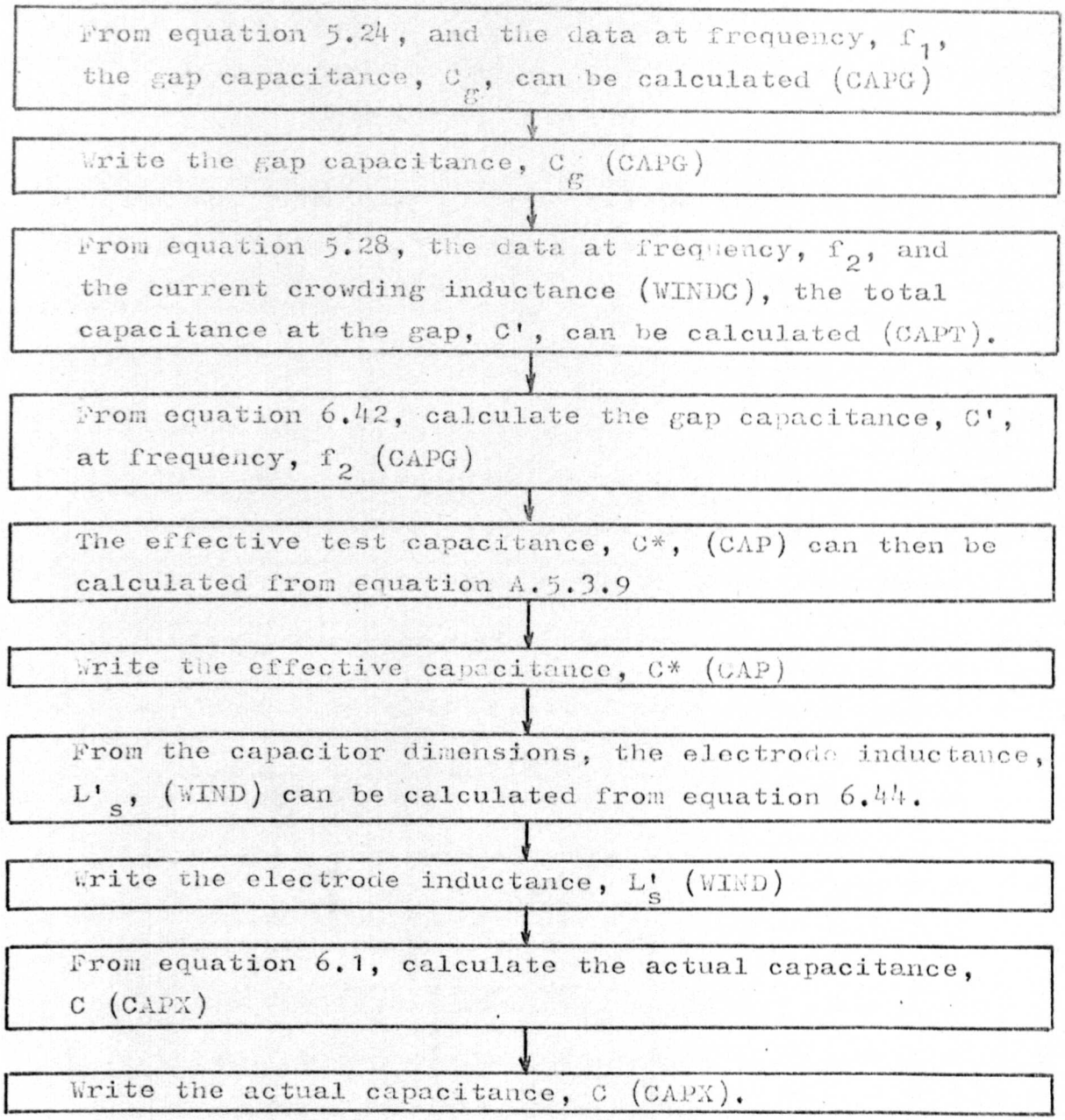
overcoupled → Calculate the coupling coefficient (BCOF2) from equation A.8.2.1 (+)

↓

Print the coupling coefficient (BCOF2)

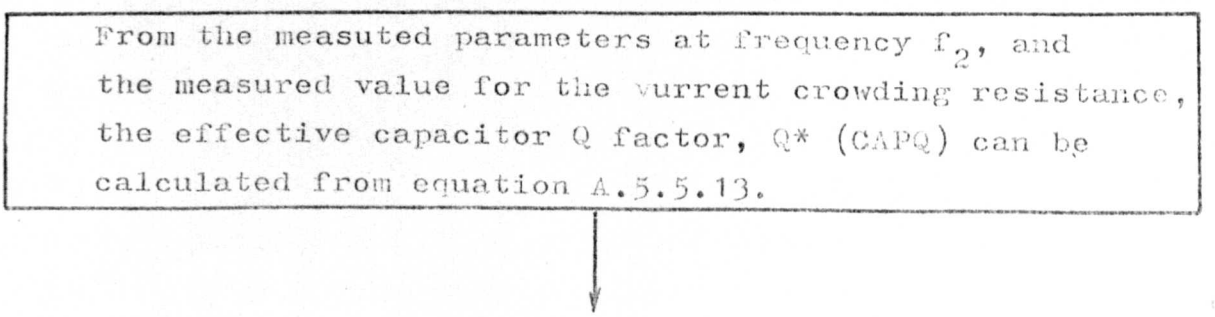
A.8.6.8 Determination of the test capacitance

Subroutine TESTC



A.8.6.9 Calculation of the capacitor Q factor from the measured return loss (RLOS2)

Subroutine BCAPQ



Write the effective capacitor Q factor, Q^* (CAPQ)

A.8.6.10 Calculation of the electrode Q factor, the dielectric Q factor, and the dielectric constant.
Subroutine COMPQ

From the estimated conductivity values, and the capacitor dimensions, calculate the electrode resistance, Rs, (RAC) from equations 6.43, and 6.45.

Calculate the electrode Q factor, Q_E^*, from equation 6.4 (ELECQ)

Write the electrode Q factor, Q_E^* (ELECQ)

Calculate the effective dielectric Q factor from equation 6.2 (DIELQ)

Write the effective dielectric Q factor, Q_D^*, (DIELQ)

Calculate the actual dielectric Q factor, Q_D, (ADILQ) from equation 6.3.

Write the actual dielectric Q factor, Q_D (ADILQ)

Calculate the dielectric constant, e_d, (ER) from equation 6.46.

Write the dielectric constant, e_d, (ER).

APPENDIX 8.7

Measurement analysis computer program - program listing

The most important of the variables used in the program are listed in Appendix 8.6.

Language - Fortran 4

```
C      CHARACTERISTIC IMPEDANCE
       SUBROUTINE IMP
       COMMON H,WI,WR,ENGOP,ENGS,TWID,WEN1,TDEP,GWID,WEN3,GDEP,BWID,WEN2,
      GBDEP,F1,Q1,F2,Q2,EFFR1,EFFR2,EFFI1,EFFI2,CONT,CONB,CCOUP,RLOS1,RL
      CS2,ZI1,ZI2,ZR1,ZR2,BCOF,BCOF1,BCOF2,CAP,CAPO,CAPG,CAPT,ENGO1,ENGO2
      C,TANDC,TRAN1,TRAN2,DELR1,DELR2,CCAP,EFFIL,EFFIH,EFFRL,EFFRH,ALPH1,
      CCAPX
       ASPR=WR/H
       ASPI=WI/H
       IF(ASPR-1)18,18,19
18     ZRW=60*ALOG(8/ASPR+ASPR/4)
19     ZRW=120*3.141593/(ASPR+2.42-0.44/ASPR+(1-1/ASPR)**6)
       IF(ASPI-1)20,20,21
20     ZIW=60*ALOG(8/ASPI+ASPI/4)
21     ZIW=120*3.141593/(ASPI+2.42-0.44/ASPI+(1-1/ASPI)**6)
       FH=1.2E+10
       FL=6.0E+09
       EFFRL=3.167
       EFFRH=3.239
       F=F1
       EFF=EFFRL+(F-FL)*((EFFRH-EFFRL)/(FH-FL))
       EFFR1=EFF
       F=F2
       EFF=EFFRL+(F-FL)*((EFFRH-EFFRL)/(FH-FL))
       EFFR2=EFF
       EFFIL=3.005
       EFFIH=3.03
       F=F1
       EFF=EFFIL+(F-FL)*((EFFIH-EFFIL)/(FH-FL))
       EFFI1=EFF
       F=F2
       EFF=EFFIL+(F-FL)*((EFFIH-EFFIL)/(FH-FL))
       EFFI2=EFF
       ZR1=ZRW/SQRT(EFFR1)
       ZR2=ZRW/SQRT(EFFR2)
       ZI1=ZIW/SQRT(EFFI1)
       ZI2=ZIW/SQRT(EFFI2)
       WRITE(2,31)ZI1,ZI2,ZR1,ZR2
31     FORMAT(21H LINE IMPEDANCE ZI1 =,F7.3/21H                    ZI2 =,F7.3
      C/21H                  ZR1 =,F7.3/21H                ZR2 =,F7.3)
       RETURN
       END
```

```
C      COUPLING COEFFICIENT B
       SUBROUTINE COUPL (RLOS)
       COMMON H,WI,WR,ENGOP,ENGS,TWID,WEN1,TDEP,CWID,WEN3,CDEP,BWID,WEN2,
      CBDEP,F1,Q1,F2,Q2,EFFR1,EFFR2,EFFI1,EFFI2,CONT,CONB,CCOUP,RLOS1,RL
      CS2,ZI1,ZI2,ZR1,ZR2,BCOF,BCOF1,BCOF2,CAP,CAP0,CAPG,CAPT,ENGO1,ENGO
      C,TANDC,TRAN1,TRAN2,DELR1,DELR2,CCAP,EFFIL,EFFIH,EFFRL,EFFRH,ALPH1,
      CCAPX
       IF(RLOS)2,3,4
3      WRITE(2,5)
5      FORMAT(20H RETURN LOSS ZERO DB)
2      BCOF=(1+EXP((ABS(RLOS)/10)*ALOG(10,0))-2*EXP((ABS(RLOS)/20)*ALOG(1
      C0,0)))/(1-EXP((ABS(RLOS)/10)*ALOG(10,0)))
       GOTO 13
4      BCOF=(1+EXP((ABS(RLOS)/10)*ALOG(10,0))+2*EXP((ABS(RLOS)/20)*ALOG(1
      C0,0)))/(1-EXP((ABS(RLOS)/10)*ALOG(10,0)))
13     BCOF=ABS(BCOF)
       WRITE(2,6)BCOF
6      FORMAT(23H COUPLING COEFFICIENT =,F8,3)
       RETURN
       END
```

```
C      CALCULATION OF J21 FROM RETURN LOSS 1
       SUBROUTINE TRANS
       COMMON H,WI,WR,ENGOP,ENGS,TWID,WEN1,TDEP,CWID,WEN3,CDEP,BWID,WEN2,
      CBDEP,F1,Q1,F2,Q2,EFFR1,EFFR2,EFFI1,EFFI2,CONT,CONB,CCOUP,RLOS1,RL
      CS2,ZI1,ZI2,ZR1,ZR2,BCOF,BCOF1,BCOF2,CAP,CAP0,CAPG,CAPT,ENGO1,ENGO2
      C,TANDC,TRAN1,TRAN2,DELR1,DELR2,CCAP,EFFIL,EFFIH,EFFRL,EFFRH,ALPH1,
      CCAPX
       CON=1E-06
       TRAN1=1E-06
53     DELR1=2,99793E8*(ATAN(SQRT(ZR1**2*TRAN1*((ZI1**2*TRAN1-1)/(ZR1**2*
      CTRAN1-1))))))/(2*3,141593*F1*SQRT(EFFR1))
       DELR1=ABS(DELR1)
       ENGO1=ENGOP+DELR1
       ANGS1=2*3,141593*F1*ENGS*(SQRT(EFFR1))/2,99793E8
       ANGO1=2*3,141593*F1*ENGO1*(SQRT(EFFR1))/2,99793E8
       TRAN3=BCOF1*(SIN(ANGO1))**2*(SIN(ANGS1)/COS(ANGS1)-COS(ANGO1)/SIN(
      CANGO1)+2*3,141593*F1*SQRT(EFFR1)*(ENGO1/(SIN(ANGO1))**2+ENGS/(COS(
      CANGS1))**2)/2,99793E8)/(2*ZI1*ZR1*Q1)
       IF(TRAN1-TRANS)102,103,104
102    TRAN1=TRAN1+CON
       GOTO 53
104    TRAN1=TRAN1-CON
       CON=CON/10
       IF(CON-1E-10)103,56,56
56     GOTO 53
103    RETURN
       END
```

```
C      COUPLING CAPACITOR DETERMINATION
       SUBROUTINE COUPC
       COMMON H,WI,WR,ENGOP,ENGS,TWID,WEN1,TDEP,CWID,WEN3,CDEP,BWID,WEN2,
```

```
      CBDEP,F1,Q1,F2,Q2,EFFR1,EFFR2,EFFI1,EFFI2,CONT,CONB,CCOUP,RLOS1,PL
      CS2,ZI1,ZI2,ZR1,ZR2,BCOF,BCOF1,BCOF2,CAP,CAPO,CAPG,CAPT,ENGO1,ENGO
      C,TANDC,TRAN1,TRAN2,DELR1,DELR2,CCAP,EFFIL,EFFIH,EFFRL,EFFRH,ALPH1
      CCAPX
       CCAP=(SQRT(TRAN1/((TRAN1*ZR1**2-1)*(TRAN1*ZI1**2-1)))/(2*3,141593
      CF1))
       WRITE(2,101)CCAP
101    FORMAT(21H COUPLING CAPACITOR =,E11,4)
       RETURN
       END




C      DETERMINATION OF LINE LENGTHS LO1,LO2
       SUBROUTINE DEL (CAPC)
       COMMON H,WI,WR,ENGOP,ENGS,TWID,WEN1,TDEP,CWID,WEN3,CDEP,BWID,WEN2
      CBDEP,F1,Q1,F2,Q2,EFFR1,EFFR2,EFFI1,EFFI2,CONT,CONB,CCOUP,RLOS1,PL
      CS2,ZI1,ZI2,ZR1,ZR2,BCOF,BCOF1,BCOF2,CAP,CAPO,CAPG,CAPT,ENGO1,ENGO
      C,TANDC,TRAN1,TRAN2,DELR1,DELR2,CCAP,EFFIL,EFFIH,EFFRL,EFFRH,ALPH1
      CCAPX
       TRAN1=(ZI1**2*ZR1**2+(1/(2*3,141593*F1*CAPC))**2-SQRT((ZI1**2+ZR1
      C*2+(1/(2*3,141593*F1*CAPC))**2)**2-4*ZI1**2*ZR1**2))/(2*ZI1**2*ZR
      C**2)
       WRITE(2,50)TRAN1
50     FORMAT(6H J21 =,E11,4)
       DELR1=2,99793E8*(ATAN(SQRT(ZR1**2*TRAN1*(ZI1**2*TRAN1-1)/(ZR1**2*
      CRAN1-1))))/(2*3,141593*F1*SQRT(EFFR1))
       ENGO1=ENGOP+DELR1
       TRAN2=(ZI2**2*ZR2**2+(1/(2*3,141593*F2*CAPC))**2-SQRT((ZI2**2+ZR2
      C*2+(1/(2*3,141593*F2*CAPC))**2)**2-4*ZI2**2*ZR2**2))/(2*ZI2**2*ZR
      C**2)
       WRITE(2,51)TRAN2
51     FORMAT(6H J22 =,E11,4)
       DELR2=2,99793E8*(ATAN(SQRT(ZR2**2*TRAN2*(ZI2**2*TRAN2-1)/(ZR2**2*
      CRAN2-1))))/(2*3,141593*F2*SQRT(EFFR2))
       ENGO2=ENGOP+DELR2
       WRITE(2,32)ENGO1
       WRITE(2,33)ENGO2
32     FORMAT(28H EFFECTIVE LINE LENGTH LO1 =,E13,5)
33     FORMAT(28H EFFECTIVE LINE LENGTH LO2 =,E13,5)
       RETURN
       END




C      TEST CAPACITOR
       SUBROUTINE TESTC
       COMMON H,WI,WR,ENGOP,ENGS,TWID,WEN1,TDEP,CWID,WEN3,CDEP,BWID,WEN2,
      CBDEP,F1,Q1,F2,Q2,EFFR1,EFFR2,EFFI1,EFFI2,CONT,CONB,CCOUP,RLOS1,PL
      CS2,ZI1,ZI2,ZR1,ZR2,BCOF,BCOF1,BCOF2,CAP,CAPO,CAPG,CAPT,ENGO1,ENGO
      C,TANDC,TRAN1,TRAN2,DELR1,DELR2,CCAP,EFFIL,EFFIH,EFFRL,EFFRH,ALPH1,
      CCAPX
       ANGS1=2*3,141593*F1*ENGS*(SQRT(EFFR1))/2,99793E8
       ANGO1=2*3,141593*F1*ENGO1*(SQRT(EFFR1))/2,99793E8
       ANGO2=2*3,141593*F2*ENGO2*(SQRT(EFFR2))/2,99793E8
       ANGS2=2*3,141593*F2*ENGS*(SQRT(EFFR2))/2,99793E8
```

```
      CAPG=1/(2*3,141593*F1*ZR1*(SIN(ANGS1)/COS(ANGS1)-COS(ANGO1)/SIN(AN
     GGO1)))
      WRITE(2,34)CAPG
34    FORMAT(21H GAP CAPACITANCE CG =,E11,4)
      CAPT=1/(2*3,141593*F2*ZR2*(SIN(ANGS2)/COS(ANGS2)-COS(ANGO2)/(SIN(A
     CNGO2))))
      CAPG=CAPG*(WR-TWID)/WR
      WINDC=0,0331E-9
      CAPTT=CAPT/(1+CAPT*WINDC*(2*3,141593*F2)**2)
      CAP=CAPTT-CAPG
      WRITE(2,35)CAP
35    FORMAT(31H EFFECTIVE TEST CAPACITANCE C =,E11,4)
      WHI=TWID/H
      IF(WHI-1)200,200,201
200   TIN=120*3,141593*WEN1/((WHI+2,42-0,44/WHI*(1-1/WHI)**6)*2,99793E8)
      GOTO 202
201   TIN=60*WEN1*(ALOG(8/WHI+4*WHI))/2,99793E8
202   WIND=TIN
      WRITE(2,112)WIND
112   FORMAT(33H ELECTRODE SERIES INDUCTANCE LS =,E11,4)
      CAPX=1/(2*3,141593*F2*(2*3,141593*F2*WIND+1/(2*3,141593*F2*CAP)))
      WRITE(2,42)CAPX
42    FORMAT(28H ACTUAL TEST CAPACITANCE C =,E11,4)
      RETURN
      END



C     CAPACITOR Q FROM RETURN LOSS 2
      SUBROUTINE QCAPQ
      COMMON H,WI,WR,ENGOP,ENGS,TWID,WEN1,TDEP,CWID,WEN3,CDEP,BWID,WEN2,
     CBDEP,F1,Q1,F2,Q2,EFFR1,EFFR2,EFFI1,EFFI2,CONT,CONB,CCOUP,RLOS1,RLO
     CS2,ZI1,ZI2,ZR1,ZR2,BCOF,BCOF1,BCOF2,CAP,CAPQ,CAPG,CAPT,ENGO1,ENGO2
     C,TANDC,TRAN1,TRAN2,DELR1,DELR2,CCAP,EFFIL,EFFIH,EFFRL,EFFRH,ALPH1,
     CCAPX
      XM1=ENGO1/(SIN(2*3,141593*F1*ENGO1*SQRT(EFFR1)/2,99793E8))**2+ENGS
     C/(COS(2*3,141593*F1*ENGS*SQRT(EFFR1)/2,99793E8))**2
      XM2=ENGO2/(SIN(2*3,141593*F2*ENGO2*SQRT(EFFR2)/2,99793E8))**2+ENGS
     C/(COS(2*3,141593*F2*ENGS*SQRT(EFFR2)/2,99793E8))**2
      DEN1=(BCOF2/BCOF1)*(XM2/XM1)*(ZI1/ZI2)*(ZR1/ZR2)**2*(TRAN1/TRAN2)*
     C(SIN(2*3,141593*F2*ENGO2*SQRT(EFFR2)/(2,99793E8))/SIN(2*3,141593*F
     C1*ENGO1*SQRT(EFFR1)/(2,99793E8)))**2*SQRT(F2/F1)
      DEN2=2*3,141593*F2*CAP*(1+CAPG/CAP)**2*TRAN2*ZR2**2*ZI2*(1/SIN(2*3
     C,141593*F2*ENGO2*SQRT(EFFR2)/(2,99793E8)))**2
      CAPQ=BCOF2/(DEN2*(1-DEN1*(1+0,0328*WR/XM2)))
      TANDC=1/CAPQ
      WRITE(2,107)CAPQ
107   FORMAT(24H EFFECTIVE CAPACITOR Q =,F8,4)
      RETURN
      END



C     COMPONENTS OF Q FACTOR
      SUBROUTINE COMPQ
      COMMON H,WI,WR,ENGOP,ENGS,TWID,WEN1,TDEP,CWID,WEN3,CDEP,BWID,WEN2,
     CBDEP,F1,Q1,F2,Q2,EFFR1,EFFR2,EFFI1,EFFI2,CONT,CONB,CCOUP,RLOS1,RLO
     CS2,ZI1,ZI2,ZR1,ZR2,BCOF,BCOF1,BCOF2,CAP,CAPQ,CAPG,CAPT,ENGO1,ENGO2
     C,TANDC,TRAN1,TRAN2,DELR1,DELR2,CCAP,EFFIL,EFFIH,EFFRL,EFFRH,ALPH1,
     CCAPX
```

```
      PHYB=2*BDEP*SQRT(3,141593**2*4,0E-07*F2*CONB)
      SINHB=(EXP(PHYB)-EXP(-PHYB))/2
      COSHB=(EXP(PHYB)+EXP(-PHYB))/2
      CORR=(SINHB+SIN(PHYB))/(COSHB-COS(PHYB))
      SDT=1/(SQRT(3,141593**2*F2*4,0E-07*CONT))
      SDB=1/(SQRT(3,141593**2*F2*4,0E-07*CONB))
      RAC=((WEN1/TWID)*(0,33*(WEN3/TWID)**0,6))*CORR/(CONT*SDT)
      ELECQ=1/(2*3,141593*F2*CAP*RAC)
      WRITE(2,105)ELECQ
105   FORMAT(21H ELECTRODE Q FACTOR =,F10,4)
      TANDD=1/CAPQ-1/ELECQ
      DIELQ=1/TANDD
      WRITE(2,106)DIELQ
106   FORMAT(32H EFFECTIVE DIELECTRIC Q FACTOR =,F8,4)
      ADILQ=DIELQ*CAP/CAPX
      WRITE(2,108)ADILQ
108   FORMAT(29H ACTUAL DIELECTRIC Q FACTOR =,F8,4)
      ER=CAPX*CDEP*3,141593*4,0E-07*(2,99793E8)**2/(WEN3*TWID)
      WRITE(2,100)ER
100   FORMAT(25H DIELECTRIC CONSTANT ER =,F8,5)
      RETURN
      END



      COMMON H,WI,WR,ENGOP,ENGS,TWID,WEN1,TDEP,CWID,WEN3,CDEP,BWID,WEN2,
     CBDEP,F1,Q1,F2,Q2,EFFR1,EFFR2,EFFI1,EFFI2,CONT,CONB,CCOUP,RLOS1,RL
     CS2,ZI1,ZI2,ZR1,ZR2,BCOF,BCOF1,BCOF2,CAP,CAPQ,CAPG,CAPT,ENGO1,ENGO
     C,TANDC,TRAN1,TRAN2,DELR1,DELR2,CCAP,EFFIL,EFFIH,EFFRL,EFFRH,ALPH1,
     CCAPX
      N=12
      N=0
24    READ(7,25)H,WI,WR,ENGOP,ENGS
25    FORMAT(5E13,5)
      READ(7,27)F1,Q1,RLOS1,F2,Q2,RLOS2
27    FORMAT(2(E14,7,F7,2,F8,3))
      READ(7,29)TWID,WEN1,TDEP
      READ(7,29)CWID,WEN3,CDEP
      READ(7,29)BWID,WEN2,BDEP
29    FORMAT(3E13,5)
      READ(7,107)CONT,CONB
107   FORMAT(2E10,3)
      WRITE(2,111)
111   FORMAT(//28H MEASUREMENTS OF RLOS1,RLOS2)
109   CALL IMP
      CALL COUPL (RLOS1)
      BCOF1=BCOF
      CALL TRANS
      CALL COUPC
      CALL DEL (CCAP)
      CALL COUPL (RLOS2)
      BCOF2=BCOF
      CALL TESTC
      CALL BCAPQ
      CALL COMPQ
      N=N+1
      IF(5-N)24,110,110
110   STOP
      END
```

APPENDIX 8.8

Measurement analysis program - print-out of typical measurement results.

The print-out listed below is produced from the measurement analysis program of Appendix 8.7, using input data obtained from practical microwave measurements of an overlay capacitor.

```
MEASUREMENTS OF RLOS1,RLOS2
LINE IMPEDANCE ZI1 = 49,909
               ZI2 = 50,014
               ZR1 = 32,188
               ZR2 = 32,321
COUPLING COEFFICIENT =   1,536
COUPLING CAPACITOR = 0,4791E-13
J21 = 0,1200E-04
J22 = 0,6699E-05
EFFECTIVE LINE LENGTH L01 =  0,61733E-02
EFFECTIVE LINE LENGTH L02 =  0,61792E-02
COUPLING COEFFICIENT =   0,970
GAP CAPACITANCE CG = 0,8020E-13
EFFECTIVE TEST CAPACITANCE C = 0,8329E-12
ELECTRODE SERIES INDUCTANCE LS = 0,4140E-11
ACTUAL TEST CAPACITANCE C = 0,8244E-12
EFFECTIVE CAPACITOR Q =124,3975
ELECTRODE Q FACTOR = 2311,4020
EFFECTIVE DIELECTRIC Q FACTOR =131,4733
ACTUAL DIELECTRIC Q FACTOR =132,8281
DIELECTRIC CONSTANT ER = 5,71381
```